CERTIFICATION

I, the undersigned, hereby certify that 1 am the translator of the accompanying certified official copy of the documents in respect to the Japanese application for a patent identified below and of the official certificate attached thereto, and certify that 1 am conversant with the English language and the following is a true translation to the best of my knowledge and belief.

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Translator's signature : S. Fushimi

Name : Shouichi Fushimi

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[Inventor]	
[Address or Domicile]	c/o Fuji Electric Co., Ltd., 1-1 Tanabeshinden, Kawasaki-ku, Kawasaki- shi, Kanagawa Prefecture
[Name]	Kazuo MATSUZAKI
[Inventor]	
[Address or Domicile]	c/o Fuji Electric Co., Ltd., 1-1 Tanabeshinden, Kawasaki-ku, Kawasaki- shi, Kanagawa Prefecture
[Name]	Naoto FUJISHIMA
[Inventor]	
[Address or Domicile]	c/o Fuji Electric Co., Ltd., 1-1 Tanabeshinden, Kawasaki-ku, Kawasaki- shi, Kanagawa Prefecture
[Name]	Akio KITAMURA
[Inventor]	
[Address or Domicile]	c/o Fuji Electric Co., Ltd., 1-1 Tanabeshinden, Kawasaki-ku, Kawasaki- shi, Kanagawa Prefecture
[Name]	Gen TADA
[Inventor]	
[Address or Domicile]	c/o Fuji Electric Co., Ltd., 1-1 Tanabeshinden, Kawasaki-ku, Kawasaki- shi, Kanagawa Prefecture
[Name]	Masaru SAITO
[Applicant]	
[Identification Number]	000005234
[Name or Title]	Fuji Electric Co., Ltd.

[Agent]
[Identification Number] 100088339
[Patent Attorney]
[Name or Title] Masaharu SHINOBE

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[Title of the Invention]

SEMICONDUCTOR DEVICE EXHIBITING HIGH BREAKDOWN VOLTAGE, THE METHOD OF MANUFACTURING THE SAME, AND METHOD OF FORMING IMPURITY DIFFUSION REGION

[Claim]

What is claimed is:

1. A semiconductor device exhibiting a high breakdown voltage, the semiconductor device comprising:

a first region of a first conductivity type;

a second region of a second conductivity type formed selectively in the surface portion of the first region;

a third region of the first conductivity type formed selectively in the surface portion of the first region;

the second region and the third region being spaced apart from each other;

a fourth region of the first conductivity type formed selectively in the surface portion of the second region;

a fifth region of the second conductivity type formed selectively in the surface portion of the first region between the second region and the third region;

a first insulation film on the fifth region;

a gate electrode above the extended portion of the second region extended between the fourth region and the first region with a gate insulation film interposed between the extended portion of the second region and the gate electrode;

a first main electrode on the fourth region;

a second main electrode on the third region; and

the fifth region comprising a plurality of portions aligned between the

second region and the third region, the impurity concentrations in the portions of the fifth region being different from each other.

2. The semiconductor device according to Claim 1, wherein the depths of the portions of the fifth region are different from each other.

3. The semiconductor device according to Claim 1, wherein the gate electrode is extended onto the first insulation film.

4. The semiconductor device according to Claim 1, wherein the first region is formed selectively in the surface portion of a semiconductor substrate of the second conductivity type.

5. The semiconductor device according to Claim 3, wherein the second region is formed not in the surface portion of the first region but selectively in the surface portion of a semiconductor substrate.

6. The semiconductor device according to any of Claims 1 through 5, wherein the impurity concentration in the portion of the fifth region on the side of the second region is higher than the impurity concentration in the portion of the fifth region on the side of the third region.

7. The semiconductor device according to any of Claims 2 through 6, wherein the depth of the portion of the fifth region on the side of the second region is deeper than the depth of the portion of the fifth region on the side of the third region.

8. The semiconductor device according to any of Claims 1 though 7, wherein the impurity concentrations in the portions of the fifth region different from each other are the concentrations of an impurity of the second conductivity type.

9. The semiconductor device according to any of Claims 1 though 7, wherein the surface impurity concentration in the fifth region of the second

conductivity type is changed by adding an impurity of the first conductivity type, the amount thereof is less than the amount of the impurity of the second conductivity type in the fifth region, and by changing the amount of the impurity of the first conductivity type.

10. A method of manufacturing a semiconductor device exhibiting a high breakdown voltage, the method comprising the steps of:

selectively forming a second region of a second conductivity type and a third region of a first conductivity type in the surface portion of a first region of the first conductivity type such that the second region and the third region are spaced apart from each other;

selectively forming a fourth region of the first conductivity type in the surface portion of the second region;

selectively forming a fifth region of the second conductivity type in the surface portion of the first region between the second region and the third region;

forming a first insulation film on the fifth region;

forming a gate electrode above the extended portion of the second region extended between the fourth region and the first region with a gate insulation film interposed between the extended portion of the second region and the gate electrode;

forming a first main electrode on the fourth region;

forming a second main electrode on the third region;

the step of selectively forming the fifth region comprising:

introducing a predetermined amount of an impurity of the second conductivity type in the intended portion of the first region, therein the fifth region is to be formed;

dividing the intended portion of the first region into a plurality of portions for the fifth region;

adding a more amount of the impurity of the second conductivity type to the portion for the fifth region nearer to the second region; and

thermally driving the impurities in the portions for the fifth region collectively.

11. A method of manufacturing a semiconductor device exhibiting a high breakdown voltage, the method comprising the steps of:

selectively forming a second region of a second conductivity type and a third region of a first conductivity type in the surface portion of a first region of the first conductivity type, the second region and the third region being spaced apart from each other;

selectively forming a fourth region of the first conductivity type in the surface portion of the second region;

selectively forming a fifth region of the second conductivity type in the surface portion of the first region between the second region and the third region;

forming a first insulation film on the fifth region;

forming a gate electrode above the extended portion of the second region extended between the fourth region and the first region with a gate insulation film interposed between the extended portion of the second region and the gate electrode;

forming a first main electrode on the fourth region;

forming a second main electrode on the third region;

the step of selectively forming the fifth region comprising:

introducing a predetermined amount of an impurity of the second conductivity type in the intended portion of the first region, therein the fifth region is to be formed;

dividing the intended portion of the first region into a plurality of portions for the fifth region;

adding a more amount of the impurity of the second conductivity type to the portion for the fifth region nearer to the second region;

introducing a more amount of an impurity of the first conductivity type to the portion for the fifth region nearer to the third region, the amount

of the impurity of the first conductivity type being less than the predetermined amount of the impurity of the second conductivity type; and

thermally driving the impurities in the portions for the fifth region collectively.

12. A method of manufacturing a semiconductor device exhibiting a high breakdown voltage, the method comprising the steps of:

selectively forming a second region of a second conductivity type and a third region of a first conductivity type in the surface portion of a first region of the first conductivity type, the second region and the third region being spaced apart from each other;

selectively forming a fourth region of the first conductivity type in the surface portion of the second region;

selectively forming a fifth region of the second conductivity type in the surface portion of the first region between the second region and the third region;

forming a first insulation film on the fifth region;

forming a gate electrode above the extended portion of the second region extended between the fourth region and the first region with a gate insulation film interposed between the extended portion of the second region and the gate electrode;

forming a first main electrode on the fourth region;

forming a second main electrode on the third region;

the step of selectively forming the fifth region comprising:

dividing the intended portion of the first region, therein the fifth region is to be formed, into a plurality of portions;

introducing a more amount of an impurity of the first conductivity type to the portion for the fifth region nearer to the third region;

introducing a predetermined amount of an impurity of the second conductivity type to the portions for the fifth region, the predetermined amount of the impurity of the second conductivity type being more than the

amount of the impurity of the first conductivity type; and

thermally driving the impurities in the portions for the fifth region collectively.

13. The method according to any of Claims 10 through 12, the method further comprising the step of extending the gate electrode onto the first insulation film.

14. The method according to any of Claims 10 through 13, the method further comprising the step of selectively forming the first region in the surface portion of a semiconductor substrate of the second conductivity type.

15. A method of forming an impurity diffusion region, the method comprising the steps of:

forming a mask for ion implantation, the mask having a first opening, the area thereof becoming wider toward a semiconductor substrate;

implanting impurity ions at least into the surface portion of the semiconductor substrate below the first opening of the mask; and

thermally driving the implanted impurity ions, whereby to form the impurity diffusion region in the semiconductor substrate.

16. The method according to Claim 15, wherein the step of forming comprises laminating a plurality of layers on the semiconductor substrate, and etching the layers one by one from the uppermost layer to the lowermost layer using the upper layer as a mask for etching the lower layer, whereby to form a wider opening in the lower layer.

17. The method according to Claim 15, the method comprising the steps of:

forming an oxide film on a semiconductor substrate;

coating a photoresist on the oxide film;

positioning a photomask on the photoresist;

selectively forming a second opening in the photoresist through the

photomask;

removing the portion of the oxide film beneath the second opening of the photoresist and the portion of the oxide film in a predetermined lateral range from the edge of the second opening of the photoresist using the photoresist as a mask;

implanting impurity ions through the second opening of the photoresist, the oxide film and the photoresist, whereby to implant the impurity ions into the surface portion of the semiconductor substrate beneath the second opening of the photoresist, the surface portion of the semiconductor substrate beneath the photoresist but not covered by the oxide film and the surface portion of the semiconductor substrate beneath the oxide film; and

thermally driving the implanted impurity ions, whereby to form the impurity diffusion region in the semiconductor substrate.

18. The method according to Claim 15, the method comprising the steps of:

forming an oxide film on a semiconductor substrate;

forming a nitride film on the oxide film;

coating a photoresist on the nitride film;

curing the photoresist;

selectively forming a third opening in the photoresist by photolithography;

removing the portion of the nitride film beneath the third opening of the photoresist, whereby to form a fourth opening in the nitride film;

removing the portion of the oxide film beneath the fourth opening of the nitride film and the portion of the oxide film in a predetermined lateral range from the edge of the fourth opening of the nitride film using the nitride film as a mask, whereby to form a fifth opening in the oxide film;

implanting boron ions into the entire surface portion of the semiconductor substrate using the photoresist, the nitride film and the oxide

film as a mask;

removing the mask formed of the photoresist, the nitride film and the oxide film; and

thermally driving the implanted boron ions, whereby to form the impurity diffusion region in the semiconductor substrate.

19. A method of forming impurity diffusion regions, the method comprising the steps of:

forming an oxide film on a semiconductor substrate;

forming a nitride film on the oxide film;

coating a photoresist on the nitride film;

positioning a photomask on the photoresist;

selectively forming an opening in the photoresist through the photomask;

removing the portion of the nitride film beneath the opening of the photoresist and the portion of the nitride film in a predetermined lateral range from the edge of the opening of the photoresist using the photoresist as a mask;

implanting impurity ions of a first conductivity type into the semiconductor substrate using the photoresist as a mask;

removing the photoresist;

thermally treating the portion of the oxide film not covered by the nitride film, whereby to form a selectively oxidized film;

removing the nitride film;

implanting impurity ions of a second conductivity type into the semiconductor substrate using the selectively oxidized film as a mask; and

thermally driving the implanted impurity ions of the first conductivity type and the implanted impurity ions of the second conductivity type, whereby to form an impurity diffusion region of the first conductivity type and an impurity diffusion region of the second conductivity type in the semiconductor substrate.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

The present invention relates to lateral semiconductor devices exhibiting a high breakdown voltage used in high-breakdown-voltage power IC's for switching power supplies, for driving motors, or for driving inverters for fluorescent lamps.

[0002]

[Prior Art]

Recently, PWM (pulse width modulation) control has been widely used for controlling switching power supplies, for driving motors, and for driving inverters for fluorescent lamps. In association with this, PWM control circuits, which exhibit excellent performances, which are small in size, which are manufactured with reduced costs, which are very reliable, and which consume less electric power, are required. To meet the requirements described above, the needs for power IC's, therein power semiconductor devices exhibiting a high breakdown voltage are integrated, are increasing. Since the power IC's drive the transformer in a power supply of 100 V or 200 V, it is necessary for the semiconductor devices in the power IC to exhibit a breakdown voltage of 700 V. To integrate the semiconductor devices easily with their control means, it is necessary to employ lateral semiconductor devices, the substrate and the drift region thereof are highly resistive (lightly doped) as disclosed in The Institute of Electronic Engineers of Japan EDD-93-21, pp. 21-29 (1993) and U.S. Patent Specification 5,452,370.

[0003]

FIG. 21 is a cross sectional view of a conventional semiconductor device exhibiting a high breakdown voltage. Referring now to FIG. 21, an n-type well region 172 is formed in a p-type substrate 171 with high resistivity of around 150 Ω cm. A p-type base region 173 is formed in n-type well region 172. The surface impurity concentration (hereinafter referred to as the

"surface concentration") in n-type well region 172 is 3 x 10^{16} cm^{-3} and the diffusion depth of n-type well region 172 is 6 μ m. The surface concentration in p-type base region 173 is 3 x 10^{16} cm^{-3} and the diffusion depth of p-type base region 173 is 2 μ m. The surface concentration of the p-type base region determines the threshold voltage of the power MOSFET.

[0004]

A p-type diffusion layer 179 (that works as a p-type offset region) is formed in the surface portion of an n-type drift region (Ld section). The p-type diffusion layer 179 is 1 μ m in depth. The surface concentration of p-type diffusion layer 179 is 5 x 10^{16} cm^{-3}. Then, an insulation film 180 formed of a thermal oxide film is formed on p-type diffusion layer 179. Insulation film 180 is 0.6 μ m in thickness. A gate electrode 177 made of polysilicon is formed above p-type base region 173 with a gate oxide film 183 of 25 nm in thickness interposed therebetween. Not shown n^+-type contact regions, 0.2 μ m in diffusion depth, are formed in an n-type source region 175 and an n-type drain region 174. The surface concentration of the n^+-type contact region is 1 x 10^{20} cm^{-3}. A p^+-type contact region 176 for securing contact is formed in the surface portion of p-type base region 173. (The surface concentration of p^+-type contact region 176 is 5 x 10^{19} cm^{-3} and the diffusion depth of p^+-type contact region 176 is 0.5 μ m.) A not shown interlayer insulation film is formed. Contact holes are bored through the interlayer insulation film. A source electrode 181 and a drain electrode 182 are formed. Insulation film 180, formed e.g. of a LOCOS film, is formed on n-type well region 179, and gate electrode 177 is extended onto insulation film 180. In this structure, the total donor amount in n-type well region 172 below p-type diffusion layer 179 is 1 x 10^{12} cm^{-2}. A high breakdown voltage is obtained by optimizing the total donor amount in n-type well region 172, the specific resistance of p-type substrate 171, the impurity concentration in p-type diffusion layer 179, and the width Ld of the n-type drift region. The structure is effective to reduce

the on-resistance by increasing the impurity concentration in n-type well region 172 while optimizing the respective impurity concentrations in p-type diffusion layer 179 and n-type well region 172 independently.

[0005]

Now the conventional steps for forming p-type diffusion layer 179 will be briefly described below. The p-type diffusion layer 179 is a p-type impurity diffusion region described below.

FIG. 22(a) is a cross sectional view for explaining the conventional ion implantation step for forming a p-type impurity diffusion region. FIG. 22(b) is a cross sectional view for explaining the conventional thermal diffusion step for forming the impurity diffusion region.

A photoresist 52 that will work as a mask for ion implantation is formed on an n-type silicon substrate 51. A not shown photomask is positioned on photoresist 52 and photoresist 52 is patterned through the not shown photomask to obtain a mask having an opening, through that ions are implanted. Then, boron ion irradiation 55 is conducted over the entire surface of the silicon substrate. Boron ions 54 are implanted through the opening of photoresist 52 into a diffusion region 53 (cf. FIG. 22(a)). Then, photoresist 52 is removed. The implanted boron ions 54 are activated thermally and diffused thermally into silicon substrate 51, resulting in a p-type region 56 (FIG. 22(b)). Alternatively, an SiO_2 film may be used in substitution for photoresist 52 as a mask for the ion implantation. In this case, it is necessary to prepare a sheet of photomask (that is a sheet of glass pattered with emulsion or chromium) for forming a mask for ion implantation.

[0006]

FIG. 23 is a cross sectional view of a conventional lateral power MOSFET exhibiting a high breakdown voltage and including the impurity diffusion region described with reference to FIGs. 22(a) and 22(b). The operations of the conventional lateral power MOSFET will be described below also with reference to FIG. 23.

The lateral power MOSFET of FIG. 23 exhibits a breakdown voltage of 700 V or higher. When a gate signal of +5 V is applied to a gate electrode 608, a channel is created in a p-type base region 603 beneath a gate electrode. Electrons flow from an n-type source region 604 to an n-type drift region (n-type substrate 601) via the channel. The electrons are absorbed into an n-type drain region 605, resulting in an ON-state of the device. When the gate signal is removed, a reverse bias voltage is applied across the pn-junction plane between p-type base region 603 and the n-type base region (n-type silicon substrate 601) and the pn-junction plane between the n-type base region (n-type silicon substrate 601) and a p-type offset region 602 such that a certain breakdown voltage is secured by the entire structure of the device. In FIG. 23, a p-type contact region 606, a gate oxide film 607, an insulation film 609, a source electrode 610, and a drain electrode 611 are shown.

[0007]

[Problems to be solved by the Present Invention]

FIG. 24 shows an electric field strength distribution (a) in the cross section (b) of the conventional semiconductor device exhibiting a high breakdown voltage shown in FIG. 21. When n-type well region 172 in FIG. 21 is heavily doped to reduce the on-voltage, remarkable electric field localization is caused on the side of the source electrode as shown in (a) of FIG. 24. Since p-type diffusion layer 170 is extended toward the drain electrode, remarkable electric field localization is caused also in the drain side surface (cf. (a) of FIG. 24). Due to the electric field localization described above, the electric field strength E_A at the location A or the electric field strength E_B at the location B on the boundary of the oxide film exceeds 3 x 10^5 V/cm, causing breakdown at the location A or B. In the structure, in which the breakdown voltage thereof is determined by the surface structure, the breakdown voltage is affected by the parasitic charges on the boundary of the oxide film and in the oxide film and by the external parasitic charges on the device surface, making the breakdown voltage unstable. When the device

is molded with a resin, more intense electric field localization is caused by the moveable ions in the mold resin, deteriorating the breakdown voltage in some cases. Since the margin of the implanted ion dose amounts in n-type well region 172 and p-type diffusion layer 179 for the breakdown voltage is small, a low breakdown voltage is caused by the deviations of the implanted ion dose amounts.

[0008]

In view of the foregoing, it is a first object of the invention to provide a semiconductor device exhibiting a high breakdown voltage, that is manufactured with low manufacturing costs. It is a second object of the invention to provide a semiconductor device, that obviates the problems described above and facilitates stabilizing the high breakdown voltage thereof. It is a third object of the invention to provide the method of manufacturing the semiconductor device exhibiting a high breakdown voltage. It is a fourth object of the invention to provide a method of forming an impurity diffusion region applicable to the semiconductor device exhibiting a high breakdown voltage.

[0009]

[Means for solving the Problems]

According to a first aspect of the invention, there is provided a semiconductor device exhibiting a high breakdown voltage, the semiconductor device including: a first region of a first conductivity type (e.g. n-type well region); a second region of a second conductivity type (p-type base region) formed selectively in the surface portion of the first region (n-type well region); a third region of the first conductivity type (n-type drain region) formed selectively in the surface portion of the first region (n-type well region); the second region (p-type base region) and the third region (n-type drain region) being spaced apart from each other; a fourth region of the first conductivity type (n-type source region) formed selectively in the surface portion of the second region (p-type base region); a fifth region of the second

conductivity type (p-type offset region: p-type diffusion layer) formed selectively in the surface portion of the first region (n-type well region) between the second region (p-type base region) and the third region (n-type drain region); a first insulation film (LOCOS oxide film and such a thermal oxide film) on the fifth region (p-type offset region); a gate electrode above the extended portion of the second region (p-type base region) extended between the fourth region (n-type source region) and the first region (n-type well region) with a gate insulation film interposed between the extended portion of the second region (p-type base region) and the gate electrode; a first main electrode (source electrode) on the fourth region (n-type source region); a second main electrode (drain electrode) on the third region (n-type drain region); and the fifth region (p-type offset region) including a plurality of portions aligned between the second region and the third region, the impurity concentrations in the portions of the fifth region being different from each other.

[0010]

Advantageously, the depths of the portions of the fifth region are different from each other.

Advantageously, the gate electrode is extended onto the first insulation film (thermal oxide film).

Advantageously, the first region is formed selectively in the surface portion of a semiconductor substrate of the second conductivity type (p-type substrate).

Advantageously, the second region is formed not in the surface portion of the first region but selectively in the surface portion of the semiconductor substrate.

[0011]

Advantageously, the impurity concentration in the portion of the fifth region on the side of the second region is higher than the impurity concentration in the portion of the fifth region on the side of the third region.

Advantageously, the depth of the portion of the fifth region on the side of the second region is deeper than the depth of the portion of the fifth region on the side of the third region.

Advantageously, the impurity concentrations in the portions of the fifth region different from each other are the concentrations of an impurity of the second conductivity type.

[0012]

Advantageously, the surface impurity concentration in the fifth region of the second conductivity type is changed by adding an impurity of the first conductivity type, the amount thereof is less than the amount of the impurity of the second conductivity type in the fifth region, and by changing the amount of the impurity of the first conductivity type.

The electric field strength is relaxed by forming the p-type offset region of a plurality of portions, the impurity concentrations and the depths thereof are different from each other, respectively. The extended portion of the gate electrode extended onto the thermal oxide film works as a field plate, which facilitates relaxing the electric field strength around the extended portion of the gate electrode.

[0013]

According to a second aspect of the invention, there is provided a method of manufacturing a semiconductor device exhibiting a high breakdown voltage, the method including the steps of: selectively forming a second region of a second conductivity type (p-type base region) and a third region of a first conductivity type (n-type drain region) in the surface portion of a first region of the first conductivity type (e.g. n-type well region) such that the second region (p-type base region) and the third region (n-type drain region) are spaced apart from each other; selectively forming a fourth region of the first conductivity type (n-type source region) in the surface portion of the second region (p-type base region); selectively forming a fifth region of the second conductivity type (p-type offset region) in the surface portion of the first region (n-type well region) between the second region (p-type base

region) and the third region (n-type drain region); forming a first insulation film (thermal oxide film) on the fifth region (p-type offset region); forming a gate electrode above the extended portion of the second region (p-type base region) extended between the fourth region (n-type source region) and the first region (n-type well region) with a gate insulation film interposed between the extended portion of the second region (p-type base region) and the gate electrode; forming a first main electrode (source electrode) on the fourth region (n-type source region); forming a second main electrode (drain electrode) on the third region (n-type drain region); the step of selectively forming the fifth region (p-type offset region) including: introducing a predetermined amount of an impurity of the second conductivity type (p-type impurity) in the intended portion of the first region (n-type well region), therein the fifth region (p-type offset region) is to be formed; dividing the intended portion of the first region (n-type well region) into a plurality of portions for the fifth region (p-type offset region); adding a more amount of the impurity of the second conductivity type (p-type impurity) to the portion for the fifth region (p-type offset region) nearer to the second region (p-type base region); and thermally driving (annealing) the impurities in the portions for the fifth region (p-type offset region) collectively.

[0014]

According to a third aspect of the invention, there is provided a method of manufacturing a semiconductor device exhibiting a high breakdown voltage, the method including the steps of: selectively forming a second region of a second conductivity type and a third region of a first conductivity type in the surface portion of a first region of the first conductivity type, the second region and the third region being spaced apart from each other; selectively forming a fourth region of the first conductivity type in the surface portion of the second region; selectively forming a fifth region of the second conductivity type in the surface portion of the first region between the second region and the third region; forming a first insulation film on the fifth region; forming a gate electrode above the extended portion of the second

region extended between the fourth region and the first region with a gate insulation film interposed between the extended portion of the second region and the gate electrode; forming a first main electrode on the fourth region; forming a second main electrode on the third region; the step of selectively forming the fifth region including: introducing a predetermined amount of an impurity of the second conductivity type in the intended portion of the first region, therein the fifth region is to be formed; dividing the intended portion of the first region into a plurality of portions for the fifth region; adding a more amount of the impurity of the second conductivity type to the portion for the fifth region nearer to the second region; introducing a more amount of an impurity of the first conductivity type (n-type impurity) to the portion for the fifth region nearer to the third region, the amount of the impurity of the first conductivity type being less than the predetermined amount of the impurity of the second conductivity type; and thermally driving the impurities in the portions for the fifth region collectively.

[0015]

According to a fourth aspect of the invention, there is provided a method of manufacturing a semiconductor device exhibiting a high breakdown voltage, the method including the steps of: selectively forming a second region of a second conductivity type and a third region of a first conductivity type in the surface portion of a first region of the first conductivity type, the second region and the third region being spaced apart from each other; selectively forming a fourth region of the first conductivity type in the surface portion of the second region; selectively forming a fifth region of the second conductivity type in the surface portion of the first region between the second region and the third region; forming a first insulation film on the fifth region; forming a gate electrode above the extended portion of the second region extended between the fourth region and the first region with a gate insulation film interposed between the extended portion of the second region and the gate electrode; forming a first main electrode on the fourth region; forming a second main electrode on the

third region; the step of selectively forming the fifth region including: dividing the intended portion of the first region, therein the fifth region is to be formed, into a plurality of portions; introducing a more amount of an impurity of the first conductivity type to the portion for the fifth region nearer to the third region; introducing a predetermined amount of an impurity of the second conductivity type to the portions for the fifth region, the predetermined amount of the impurity of the second conductivity type being more than the amount of the impurity of the first conductivity type; and thermally driving the impurities in the portions for the fifth region collectively.

Advantageously, the gate electrode is extended onto the first insulation film.

[0016]

Advantageously, the first region is formed selectively in the surface portion of a semiconductor substrate of the second conductivity type.

According to a fifth aspect of the invention, there is provided a method of forming an impurity diffusion region (such as the p-type offset region described above), the method including the steps of: forming a mask for ion implantation, the mask having a first opening, the area thereof becoming wider toward a semiconductor substrate; implanting impurity ions at least into the surface portion of the semiconductor substrate (or the n-type well region) below the first opening of the mask; and thermally driving the implanted impurity ions to form the impurity diffusion region in the semiconductor substrate (or the n-type well region).

Advantageously, the step of forming an impurity diffusion region includes the step of: laminating a plurality of layers on the semiconductor substrate, and etching the layers one by one from the uppermost layer to the lowermost layer using the upper layer as a mask for etching the lower layer to form a wider opening in the lower layer.

[0017]

Advantageously, the method of forming an impurity diffusion region includes the steps of: forming an oxide film on a semiconductor substrate; coating a photoresist on the oxide film; positioning a photomask on the photoresist; selectively forming a second opening in the photoresist through the photomask; removing the portion of the oxide film beneath the second opening of the photoresist and the portion of the oxide film in a predetermined lateral range from the edge of the second opening of the photoresist using the photoresist as a mask; implanting impurity ions through the second opening of the photoresist, the oxide film and the photoresist to implant the impurity ions into the surface portion of the semiconductor substrate beneath the second opening of the photoresist, the surface portion of the semiconductor substrate beneath the photoresist but not covered by the oxide film and the surface portion of the semiconductor substrate beneath the oxide film; and thermally driving the implanted impurity ions to form the impurity diffusion region in the semiconductor substrate.

[0018].

Advantageously, the method of forming an impurity diffusion region includes the steps of: forming an oxide film on a semiconductor substrate; forming a nitride film on the oxide film; coating a photoresist on the nitride film; curing the photoresist; selectively forming a third opening in the photoresist by photolithography; removing the portion of the nitride film beneath the third opening of the photoresist to form a fourth opening in the nitride film; removing the portion of the oxide film beneath the fourth opening of the nitride film and the portion of the oxide film in a predetermined lateral range from the edge of the fourth opening of the nitride film using the nitride film as a mask to form a fifth opening in the oxide film; implanting boron ions into the entire surface portion of the semiconductor substrate using the photoresist, the nitride film and the oxide film as a mask; removing the mask formed of the photoresist, the nitride film and the oxide film; and thermally driving the implanted boron ions to

form the impurity diffusion region in the semiconductor substrate.

[0019]

According to a sixth aspect of the invention, there is provided a method of forming impurity diffusion regions, the method including the steps of: forming an oxide film on a semiconductor substrate; forming a nitride film on the oxide film; coating a photoresist on the nitride film; positioning a photomask on the photoresist; selectively forming an opening in the photoresist through the photomask; removing the portion of the nitride film beneath the opening of the photoresist and the portion of the nitride film in a predetermined lateral range from the edge of the opening of the photoresist using the photoresist as a mask; implanting impurity ions of a first conductivity type into the semiconductor substrate using the photoresist as a mask; removing the photoresist; thermally treating the portion of the oxide film not covered by the nitride film to form a selectively oxidized film; removing the nitride film; implanting impurity ions of a second conductivity type into the semiconductor substrate using the selectively oxidized film as a mask; and thermally driving the implanted impurity ions of the first conductivity type and the implanted impurity ions of the second conductivity type to form an impurity diffusion region of the first conductivity type and an impurity diffusion region of the second conductivity type in the semiconductor substrate.

[0020]

[Modes for carrying out the Invention]

Now the invention will be explained hereinafter with reference to the accompanied drawing figures which illustrate the preferred embodiments of the invention.

The semiconductor device according to the invention includes, as shown in FIG. 19, a p-type region (p-type offset region) 57 including a plurality of portions, the impurity concentrations therein are different from each other, in substitution for p-type region 602 (p-type offset region) shown in FIG. 23,

the impurity concentration distribution and the depth thereof are uniform. The semiconductor device according to the invention, that includes p-type region 57 described above, facilitates preventing electric field localization from causing. In FIG. 19, p-type region 57 includes three portions I, II and III, the impurity concentrations thereof are different from each other. The portions, the impurity concentrations thereof are different from each other, are formed by the following two methods.

[0021]

Although not illustrated, a first method repeats ion implantation as shown in FIG. 22(a) multiple times with the masks changed from ion implantation to ion implantation, and, then, thermally drives all the implanted ions collectively. A second method prepares three kinds of masks (61, 62 and 63), combines the masks 61, 62 and 63 appropriately such that the local mask thickness changes stepwise between the regions B, C and D as shown in FIG. 20, and controls the dose amounts of ions 59 in one-step ion implantation 58.

[0022]

It is necessary for the first method to prepare photomasks as many as the portions, since one photomask is used for forming one portion. It is also necessary for the second method to prepare photomasks as many as the portions, since the local mask thickness is obtained by combining different masks. First, the first method will be explained more in detail below.

[0023]

FIG. 1 is a cross sectional view of a semiconductor device exhibiting a high breakdown voltage according to a first embodiment of the invention. The semiconductor device shown in FIG. 1 is a lateral MOSFET exhibiting a high breakdown voltage and including a p-type region (p-type offset region), that includes a plurality of portions, the impurity concentrations thereof are different from each other.

Referring now to FIG. 1, the lateral MOSFET includes an n-type silicon substrate 71, a p-type base region 87 in the surface portion of substrate 71,

an n-type drain region 89 in the surface portion of substrate 71, a p-type offset region 83 in the surface portion of substrate 71, an n-type source region 88 in the surface portion of p-type base region 87, and a p^+-type contact region 90 in the surface portion of p-type base region 87. The p-type offset region 83 includes a first p-type region 83a, the impurity concentration thereof is the highest and the diffusion depth thereof is the deepest, a second p-type region 83b, the impurity concentration and the diffusion depth thereof are intermediate, and a third p-type region 83c, the impurity concentration thereof is the lowest and the diffusion depth thereof is the shallowest. A gate electrode 92 is formed above the extended portion of p-type base region 87 extended between n-type source region 88 and n-type silicon substrate 71 (or p-type offset region 83) with a gate insulation film 91 interposed therebetween. An insulation film 93 is formed on gate electrode 92 and p-type offset region 83. A source electrode 94 is formed on n-type source region 88. A drain electrode 95 is formed on n-type drain region 89.

[0024]

The p-type offset region 83 is different from the conventional p-type offset region in that p-type offset region 83 is formed of the first p-type region 83a, the second p-type region 83b and the third p-type region 83c, the impurity concentrations thereof are different from each other.

Table 1 lists the impurity distribution profile in p-type offset region 83.

[0025]

Table 1

P-type regions	First p-type region	Second p-type region	Third p-type region
Surface impurity concentrations	7×10^{16} cm^{-3}	5×10^{16} cm^{-3}	3×10^{16} cm^{-3}
Diffusion depths	1.5 μ m	1.2 μ m	0.9 μ m

The surface concentration is the highest in the first p-type region 83a and the lowest in the third p-type region 83c.

FIG. 2 shows a pair of curves for comparing the distributions of electric field strength in the conventional p-type offset region and p-type offset region

83 including a plurality of p-type regions, the impurity concentrations thereof are different from each other.

[0026]

When the conventional device shown in FIG. 23 is in the OFF-state, the electric field strength is abnormally high at both ends of p-type offset region 602. When the device according to the first embodiment shown in FIG. 1 is in the OFF-state, the electric field strength is rather uniform across p-type offset region 83, resulting in an improved reliability of the breakdown voltage of the device.

Then, the method of forming the p-type offset region described with reference to FIG. 1 and including a plurality of p-type layers, the impurity concentrations thereof are different from each other, will be explained below.

[0027]

FIGs. 3 through 12 are cross sectional views for explaining the manufacturing steps according to a second embodiment of the invention for forming a p-type offset region (impurity diffusion region) including a plurality of p-type layers, the impurity concentrations thereof are different from each other, in a semiconductor device exhibiting a high breakdown voltage.

A photoresist 74a is coated on n-type silicon substrate 71. An ultraviolet ray 701 is irradiated through a photomask 700. Then, an opening 75 is formed through photoresist 700 by etching (cf. FIG. 3).

[0028]

Boron ion implantation 77 is conducted at a high dose amount to implant boron ions 76 into n-type silicon substrate (cf. FIG. 4).

Then, photoresist 74a is removed from n-type silicon substrate 71, a photoresist 74b is coated on n-type silicon substrate 71, an ultraviolet ray 703 is irradiated through a photomask 702, and an opening 78 is formed through photoresist 74b by etching (cf. FIG. 5).

[0029]

Then, boron ion implantation 79 is conducted at an intermediate dose amount to implant boron ions 80 into n-type silicon substrate 71 (cf. FIG. 6).

Then, photoresist 74b is removed from n-type silicon substrate 71, a photoresist 74c is coated on n-type silicon substrate 71, an ultraviolet ray 705 is irradiated through a photomask 704, and an opening 81 is formed through photoresist 74c by etching (cf. FIG. 7).

[0030]

Then, boron ion implantation 82 is conducted at a low dose amount to implant boron ions 81 into n-type silicon substrate 71 (cf. FIG. 8).

Then, the implanted boron ions are thermally driven to form p-type region 83 including three regions, the impurity concentrations thereof are different from each other. The p-type region 83 will be a p-type offset region (cf. FIG. 9).

Then, a photoresist 84 is coated on n-type silicon substrate 71 and p-type region 83, an ultraviolet ray 708 is irradiated through a photomask 707, and an opening 85 is formed through photoresist 84 by etching (cf. FIG. 10).

[0031]

Then, boron ion implantation 87 is conducted at a high dose amount to implant boron ions 86 into n-type silicon substrate 71 (cf. FIG. 11).

Then, the implanted boron ions are thermally driven to form p-type region 87, that will be a p-type base region (cf. FIG. 12).

Then, the lateral MOSFET exhibiting a high breakdown voltage shown in FIG. 1 is completed through not shown additional manufacturing steps.

[0032]

For forming a p-type offset region including three p-type regions, the impurity concentrations thereof are different from each other, it is necessary to prepare three photomasks 700, 702 and 704, to conduct three photolithographic steps and to conduct three ion implantation steps at the respective dose amounts.

Then, the method of manufacturing a semiconductor device exhibiting a high breakdown voltage will be explained below in detail.

FIG. 13 is a cross sectional view of a semiconductor device exhibiting a high breakdown voltage according to a third embodiment of the invention. Referring now to FIG. 13, an n-type well region 152 is formed in the surface portion of a p-type substrate 151 with high resistivity of 150 Ω cm. A p-type base region 153 is formed in the surface portion of n-type well region 152. The surface concentration of n-type well region 152 is 3×10^{16} cm^{-3}. The diffusion depth of n-type well region 152 is 6 μ m. After a p-type diffusion layer 159 described later is formed, the total donor amount in n-type well region 152 is 1×10^{12} cm^{-3}. A p-type diffusion layer 158 (corresponding to p-type region 87 in FIG. 1) is formed in the surface portion of an n-type drift region (the Ld section of n-type well region 152). (When the breakdown voltage is 700 V, Ld = 70 μ m.) The p-type diffusion layer 159 is divided into a region 159a in the Lp_1 section of p-type diffusion layer 159, a region 159b in the Lp_2 section of p-type diffusion layer 159, and a region 159c in the Lp_3 section of p-type diffusion layer 159 (corresponding to the first p-type region, the second p-type region, and the third p-type region of FIG. 1, respectively). For example, the width of the Lp_1 section is 25 μ m, the width of the Lp_2 section is 20 μ m, and the width of the Lp_3 section is 25 μ m. For example, the surface concentration in the Lp_1 section is set higher by about 10 % than that in the Lp_2 section and the surface concentration in the Lp_3 section is set lower by about 10 % than that in the Lp_2 section. In detail, the surface concentration in the Lp_1 section is 5.5×10^{16} cm^{-3}, the surface concentration in the Lp_2 section is 5.0×10^{16} cm^{-3}, and the surface concentration in the Lp_3 section is 4.5×10^{16} cm^{-3}.

[0033]

In the actual manufacturing process, boron ions are implanted to the region including the sections Lp_1, Lp_2 and Lp_3 so that the surface boron concentration may be 5.0×10^{16} cm^{-3} after heat treatment (the depth after thermally treating the implanted boron atoms is indicated by the dotted line 158). Boron ions are added to the Lp_1 section so that the added surface boron

concentration in the Lp_1 section may be 0.5×10^{16} cm^{-3} after heat treatment. Phosphorus ions are doped to the Lp_3 section to compensate the boron concentration so that the doped surface phosphorus concentration in the Lp_1 section may be 0.5×10^{16} cm^{-3} after heat treatment. Since the thermal drive steps are conducted under the same conditions for the sake of simplicity, the diffusion depth is 1.1 μ m for Lp_1 section, 1.0 μ m for Lp_2 section, and 0.9 μ m for Lp_3 section. Thus, the surface concentrations and the diffusion depths of the regions 159a, 159b, and 159c are adjusted precisely by doping a certain amount of boron ions in advance and by doping an additional amount of boron ions or phosphorus ions. The surface concentration in p-type base region 153 is 3×10^{16} cm^{-3}. The diffusion depth of the p-type base region 153 is 2 μ m. The threshold voltage of the power MOSFET is set by the surface concentration in p-type base region 153. As described above, the surface concentrations and the diffusion depths of the regions 159a, 159b, and 159c constituting p-type diffusion layer 159 are adjusted precisely by doping a certain amount of boron ions in advance and by doping an additional amount of boron ions or phosphorus ions. Alternatively, the p-type region including a plurality of regions, the surface concentration and the diffusion depths thereof are different from each other, may be formed only by implanting boron ions, although the precision of forming is not so good.

[0034]

Then, a thermal oxide film (an insulation film 160 and such a LOCOS film) of 0.6 μ m in thickness is formed. A polysilicon gate electrode 157 is formed on a gate oxide film 163 of 25 nm in thickness. (The symbol L in FIG. 13 designates the channel region.) Although not shown in FIG. 13, n^+-type contact regions are formed in an n-type source region 155 and an n-type drain region 154. The surface concentration of the n^+-type contact regions is 1×10^{20} cm^{-3}. The diffusion depth of the n^+-type contact regions is 0.2 μ m. A p^+-type contact region 156 for securing contact is formed in the surface portion of p-type base region 153. (The surface concentration of p^+-type

contact region 156 is 5 x 10^{19} cm^{-3}. The diffusion depth of p^+-type contact region 156 is 0.5 μ m.) A not shown interlayer insulation film is formed. Contact holes are bored. And, a source electrode 161 and a drain electrode 162 are formed.

[0035]

Various alternative methods may be employed to provide p-type diffusion layer 159 with various concentration distribution profiles. The number of regions in p-type diffusion layer 159 is not limited to 3 (regions 159a, 159b, and 159c). The number of the regions in p-type diffusion layer 159 varies depending on the breakdown voltage class, the thermal oxide film thickness, the state of mounting, the circumstances in that the device is used, and such conditions. It is not always necessary to cover p-type base region 153 with n-type well region 152. The structure including an n-type well region terminated by the channel region (L section) (the structure in that n-type well region 152 is in contact with p-type base region 153 across the surfaces thereof) operates properly as intended.

[0036]

It has been confirmed by simulation that the electric field strength distributes as illustrated in (a) of FIG. 14 across the semiconductor structure described above. The electric field strengths E_C, E_D, E_E and E_F at the points C, D, E and F are lower than 2 x 10^5 V/cm. The electric field strength is low at these points due to the depletion layer expanding from the pn-junction between p-type base region 153 and n-type well region 152 to n-type well region 152 and the depletion layer expanding from the pn-junction between n-type well region 152 and p-type diffusion layer 159 to the portion of p-type diffusion layer 159 in the vicinity of n-type drain region 154. Breakdown is determined by the junction portion (point G) between n-type well region 152 and p-type substrate 151 below n-type drain region 154.

[0037]

The structure described above facilitates securing a stable breakdown

voltage at a high temperature and under application of a high voltage for a long period of time. Since the n-type well region 152 below p-type diffusion layer 159c, that causes the most part of the on-resistance, is enlarged according to the invention as compared with that in the conventional semiconductor structure, the on-resistance is reduced. When n-type well region 152 is formed by diffusion, the heavily doped region is expanded and the on-resistance is reduced by 5 % as compared with that in the conventional semiconductor structure.

[0038]

FIG. 15 is a cross sectional view of a semiconductor device exhibiting a high breakdown voltage according to a fourth embodiment of the invention. Referring now to FIG. 15, the semiconductor device according to the fourth embodiment includes a p-type substrate 151 with high resistivity of 150 Ω cm, an n-type well region 164 in the surface portion of p-type substrate 151, and a p-type base region 153 in the surface portion of n-type well region 164. The p-type well region 164 includes a first well region 165, a second well region 166 and a third well region 167, the impurity concentrations thereof are different from each other. The surface concentration is 2.4×10^{16} cm^{-3} for first well region 165, 3.0×10^{16} cm^{-3} for second well region 166, and 3.6×10^{16} cm^{-3} for third well region 167. The diffusion depth is from 4 μ m to 6 μ m. For example, the width Lp_1 is about 25 μ m, the width Lp_2 is about 20 μ m, and the width Lp_3 is about 25 μ m. A p-type diffusion layer 169 including three p-type regions, the surface concentrations and the diffusion depths thereof are different from each other, is formed in the surface portion of an n-type drift region (the section Ld of n-type well region 164). (The width of the section Ld is about 70 μ m to guarantee the breakdown voltage of 700 V.) To form p-type diffusion layer 169, boron ions are doped collectively to the diffusion depth of 1.0 μ m at the surface concentration of 5×10^{16} cm^{-3}. The boron diffusion depth is indicated by a broken line 168. As a result, a first p-type region 169a corresponds to first n-type well region 165, a second p-type

region 169b to second well region 166, and a third p-type region 169c to third well region 167.

[0039]

In the actual manufacturing process, phosphorus ions are implanted to the portion of the n-type well region including the sections Lp_1, Lp_2 and Lp_3 at the dose amount, at that the surface phosphorus concentration will be 2.4 x 10^{16} cm^{-3} after heat treatment. The implanted phosphorus ions are thermally treated (driven) at 1150 ℃ for 10 hr. Phosphorus ion are added to the sections Lp_2 and Lp_3 at the dose amount, at that the surface phosphorus concentration in the sections Lp_2 and Lp_3 will be increased by 0.6 x 10^{16} cm^{-3} after heat treatment. And, phosphorus ion are added to the section Lp_3 at the dose amount, at that the resultant surface phosphorus concentration in the section Lp_3 will be further increased by 0.6 x 10^{16} cm^{-3} after heat treatment. Then, to form p-type diffusion layer 164, boron ions are doped to the region including the sections Lp_1, Lp_2 and Lp_3 at the dose amount, at that the surface boron concentration will be 5 x 10^{16} cm^{-3} after heat treatment. The doped boron ions are treated thermally.

[0040]

The surface concentration of p-type base region 153 is 3 x 10^{16} cm^{-3}. The diffusion depth of p-type base region 153 is 2 μ m. The threshold voltage of the power MOSFET is set by the surface concentration in p-type base region 153. Then, a thermal oxide film 160 of 0.6 μ m in thickness is formed. A polysilicon gate electrode 157 is formed on a gate oxide film 163 of 25 nm in thickness. Although not shown in FIG. 15, n^+-type contact regions, the diffusion depth thereof is 0.2 μ m and the surface concentration thereof is 1 x 10^{20} cm^{-3}, are formed in an n-type source region 155 and an n-type drain region 154. In FIG. 15, a p^+-type contact region 156 is shown. (The surface concentration in the p^+-type contact region is 5 x 10^{19} cm^{-3} and the diffusion depth of the p^+-type contact region is 0.5 μ m.) Various alternative methods

may be employed to provide n-type well region 164 with a certain concentration distribution profile. The number of the regions in p-type diffusion layer 169 is not limited to three. The number of the regions in p-type diffusion layer 169 depends on the breakdown voltage class, the thermal oxide film thickness, the state of mounting, the circumstances, in that the device is used, and such conditions.

[0041]

The semiconductor device according to the fourth embodiment exhibits the same effects as that the semiconductor device according to the third embodiment does.

For forming a diffusion layer including a plurality of regions, the impurity concentrations thereof are different from each other, it is necessary to prepare multiple sheets of photomasks as many as the regions. For forming diffusion layers, the conductivity types thereof are different from each other, it is also necessary for the foregoing manufacturing methods to prepare multiple sheets of photomasks. The necessity of preparing multiple sheets of photomasks soars the manufacturing costs. The improved methods, which obviate the problem described above, form multiple impurity diffusion regions, the impurity concentrations thereof are different from each other, using one photomask.

[0042]

Now the improved methods will be described briefly. The improved methods employ one photomask to form a plurality of regions, the impurity concentrations thereof are different from each other or to form diffusion regions, the conductivity types thereof are different from each other.

One of the improved method uses a thin film formed of multiple layers, the materials and the etching speed thereof are different from each other, as a mask for ion implantation. The uppermost layer of the mask is machined using a photomask and the lower layers are machined one after another. An opening is formed through each layer of the mask for ion implantation by self-alignment so that the lower layer of the mask has a wider opening.

Regions, the implanted ion amounts thereof are different from each other, are formed in an impurity diffusion region through one step ion implantation using the mask formed as described above.

[0043]

Or, a mask for implanting ions of different conductivity types is formed by self-alignment using a photomask, and impurity diffusion regions, the conductivity types thereof are different from each other, are formed using the mask formed as described above.

Here, the word "self-alignment" means that a plurality of similar patterns is formed using one photomask.

[0044]

FIGs. 16(a) through 16(e) are cross sectional views explaining the steps for forming a plurality of impurity diffusion regions, the impurity concentrations thereof are different from each other. The impurity diffusion regions correspond to the p-type diffusion layer described above.

An SiO_2 film 42 is formed on a silicon substrate 41. A photoresist 43 is coated on SiO_2 film 42. After photoresist 43 is cured, an ultraviolet ray 45 is irradiated onto photoresist 43 through a photomask 44. An opening 46 is formed in the section of photoresist 43 corresponding to the section, therein a diffusion region is to be formed, by light exposure and by subsequent etching (cf. FIG. 16(a)). Then, the portion of SiO_2 film 42 beneath opening 46 of photoresist 43 is removed by dry etching (cf. FIG. 16(b)). Then, SiO_2 film 42 below photoresist 43 is removed for an intended lateral width (the section II in FIG, 16(c)) with hydrofluoric acid (cf. FIG. 16(c)). Thus, the section, for which silicon substrate 41 is exposed (section I), the section covered with photoresist 43 (the section II), and the section covered with SiO_2 film 42 and photoresist 43 (the section III) are formed by self-alignment using one single photomask 44.

[0045]

Then, boron ion implantation 47 onto the entire surface of silicon substrate 41 is conducted. Since the ion-implantation blocking capabilities of

the sections I, II and III are different from each other, the implanted amounts of ions 48 in the sections I, II and II are different from each other. More in detail, the following relational expression holds for the implanted ion amounts in the sections I, II and II (cf. FIG. 16(d)).

The implanted ion amount in section I > The implanted ion amount in section II > The implanted ion amount in section III

Then, a p-type region 49 is formed by removing photoresist 43 and by thermally driving the implanted ions. The p-type region 49 includes continuous impurity diffusion regions, the impurity concentrations thereof are different from each other (cf. FIG. 16(e)). Since the ranges of the ions are different from region to region, the diffusion depths of the regions are little bit different from each other. (The depths of the regions are exaggerated in FIG. 16(e)).

[0046]

Now a method of forming a plurality of impurity diffusion layers, the impurity concentrations thereof are different from each other, using one single photomask, and a method of forming a plurality of impurity diffusion layers, the conductivity types thereof are different from each other, using one single photomask will be described in connection with respective embodiments.

FIGs. 17(a) through 17(e) are cross sectional views for explaining the steps of forming a plurality of impurity diffusion regions, the impurity concentrations thereof are different from each other, according to a fifth embodiment of the invention.

The method described with reference to FIGs. 17(a) through 17(e) uses a photomask 100 to form a p-type offset region 10 formed of three p-type regions 7, 8 and 9.

[0047]

An LTO-SiO_2 film (SiO_2 film formed by low temperature oxidation) 2 of

1 μ m in thickness is formed on an n-type silicon substrate 1. A plasma SiN film (silicon nitride film formed by the plasma CVD method) 3 of 1 μ m in thickness is formed on LTO-SiO_2 film 2. A photoresist 4 of 1 μ m in thickness is coated on plasma SiN film 3. Photoresist 4 is cured, and an ultraviolet ray 101 is irradiated through a photomask 100 onto photoresist 4. After exposing photoresist 4 to the lights, an opening 16 is formed by etching in the portion of photoresist 4 corresponding to the portion, therein a diffusion region is to be formed (cf. FIG. 17(a)).

[0048]

Then, the portion of plasma SiN film 3 below opening 16 of photoresist 4 is removed by dry etching. Although not shown in the figures, SiN film 3 has a double-layered structure having an upper layer of around 5 nm in thickness, the etching speed thereof is fast. The upper layer exhibiting a high etching speed is formed by modifying the surface of SiN film 3. The surface of SiN film 3 is modified by exposing the surface of SiN film 3 to hydrogen plasma. Alternatively, the upper layer of SiN film 3 is formed by depositing a thin plasma CVD-SiN:H film (silicon nitride film containing a small amount of hydrogen formed by the plasma CVD method) on a thermal silicon nitride film SiN. Due to the upper layer exhibiting a high etching speed, SiN film 3 is etched laterally for a certain width X. The etching plane of SiN film 3 is tapered as illustrated in FIG. 17(b). The lateral width X is adjusted by prolonging the etching period of time exceeding the period of time, for which SiN film 3 is etched for the thickness thereof.

[0049]

LTO-SiO_2 film 2 is not etched by the dry etching described above. The substrate 1 is dipped in hydrofluoric acid and LTO-SiO_2 film 2 is etched for a certain lateral width Y from the edge of the opening of plasma SiN film 3 by wet etching. Then, boron ion implantation 5 onto the entire surface of silicon substrate 1 is conducted through the mask formed of photoresist 4, plasma SiN film 3 and LTO-SiO_2 film 2. The concentration of the implanted boron

ions 6 is the highest in the region A of silicon substrate 1 below opening 16 of photoresist 4. The concentration of the implanted boron ions 6 is intermediate in the region B of silicon substrate 1 below photoresist 4. The concentration of implanted boron ions 6 is the lowest in the region C of silicon substrate 1 below the double-layered mask formed of photoresist 4 and plasma SiN film 3. The concentration of the implanted boron ions 6 is zero in the region D of silicon substrate 1 below the triple-layered mask formed of photoresist 4, plasma SiN film 3 and LTO-SiO_2 film 2, since the boron ions do not reach the region D. When the triple-layered mask is thin enough, the implanted boron ions 6 may be in the region D (cf. FIG. 17(b)).

[0050]

Then, the mask for ion implantation (including photoresist 4, plasma SiN film 3 and LTO-SiO_2 film 2) is removed, and the implanted boron ions 6 are driven thermally. As a result of this thermal drive, the regions A, B and C are turned to a first p-type region 7, a second p-type region 8 and a third p-type region 9, respectively. The boron concentration is the highest in the first p-type region 7, intermediate in the second p-type region 8 and the lowest in the third p-type region 9. The first p-type region 7, the second p-type region 8 continuous to the first p-type region 7 and the third p-type region 9 continuous to the second p-type region 8 constitute a p-type region 10 (cf. FIG. 17(c)). Since the ranges of the ions are different from region to region, the diffusion depths of the regions are little bit different from each other. (The depths of the regions are exaggerated in FIG. 17(c)).

[0051]

Then, a p-type base region and a part of the p-type offset region are formed by boron ion implantation 13 using a patterned photoresist 11 as a mask. The dose amount of boron ions 12 is set to be equal to or higher than the boron dose amount in the foregoing region A (cf. FIG. 17(d)).

Then, p-type regions 14 and 15 are formed by heat treatment. The p-type region 14 is used for a p-type base region for forming a semiconductor device. The p-type region 15 and the first through third regions 7 through 9

constitute a p-type offset region with varied impurity concentrations (cf. FIG. 17(e)).

[0052]

Although the descriptions on the succeeding manufacturing steps are omitted, a semiconductor device same as the semiconductor device of FIG. 1 is obtained finally.

Thus, a plurality of impurity diffusion regions (the regions 7, 8 and 9), the impurity concentrations thereof are different from each other, is formed using one single photomask 100.

FIGs. 18(a) through 18(d) are cross sectional views for explaining the steps of forming a plurality of impurity diffusion regions, the conductivity types thereof are different from each other, according to a sixth embodiment of the invention. The method described with reference to FIGs. 18(a) through 18(d) uses a photomask to form two diffusion layers, the conductivity types thereof are different from each other.

[0053]

A thermal silicon oxide film (hereinafter referred to as an "SiO_2 film") 23 of 20 nm in thickness and, then, a thermal silicon nitride film (hereinafter referred to as an "SiN film") 24 of 20 nm in thickness are deposited on an n-type silicon substrate 21. A photoresist 25 is coated on SiN film 24 and, then, photoresist 25 is cured. Photoresist 25 is patterned by irradiating an ultraviolet ray 201 through a photomask 200 such that photoresist 25 has a window in the portion thereof corresponding to the portion of n-type silicon substrate 21, therein a diffusion region is to be formed (cf. FIG. 18(a)). Similarly as the foregoing SiN film 3, SiN film 24 has a double-layered structure having an upper layer of around 5 nm in thickness, the etching speed thereof is fast. Due to the double-layered structure, SiN film 24 below photoresist 25 is etched laterally by plasma etching through the window of photoresist 25. The lateral etching width X is adjusted by controlling the over-etching period of time.

[0054]

Then, boron ion implantation 26 is conducted to implant boron ions 27 in the portion below the window of photoresist 25 (cf. FIG. 18(b)).

Then, photoresist 25 is removed. A p^+-type region 29 is formed by thermally driving the implanted boron ions 27 in an oxidizing atmosphere. At the same time, a thick oxide film (LOCOS) 28 of around 1 μ m in thickness is formed in the portion of SiO_2 film 23 not covered by SiN film 24 (cf. FIG. 18(c)).

LOCOS 28 works as a mask for the succeeding impurity ion implantation. By phosphorus ion implantation 30, phosphorous ions 31 of the opposite conductivity type are implanted in the portion not covered by LOCOS 28 as shown in FIG. 18(c). An n^+-type region 32 is formed by the succeeding thermal drive. In short, diffusion regions (29 and 32), the conductivity types thereof are opposite to each other, are formed through the above described steps using one single photomask 200 (cf. FIG. 18(d)).

Thus, impurity diffusion regions, the conductivity types thereof are different each other, are formed using only one photomask.

[0055]

[Effect of the Invention]

As described above, the semiconductor device according to the invention, which includes an offset region including a plurality of impurity diffusion regions, the impurity concentrations thereof are different from each other, facilitates stabilizing the breakdown voltage thereof.

The manufacturing method according to the invention, that uses only one photomask for forming a plurality of impurity diffusion regions, the impurity concentrations thereof or the conductivity types thereof are different from each other, facilitates reducing the manufacturing costs.

[Brief Description of the Drawing Figures]

FIG. 1 is a cross sectional view of a semiconductor device exhibiting a

high breakdown voltage according to the first embodiment of the invention.

FIG. 2 shows a pair of curves for comparing the distributions of electric field strength in the conventional p-type offset region and the p-type offset region according to the invention including a plurality of p-type regions, the impurity concentrations thereof are different from each other.

FIG. 3 is a cross sectional view explaining a manufacturing step for manufacturing a semiconductor device exhibiting a high breakdown voltage according to the second embodiment of the invention.

FIG. 4 is a cross sectional view explaining the manufacturing step subsequent to the step of FIG. 3.

FIG. 5 is a cross sectional view explaining the manufacturing step subsequent to the step of FIG. 4.

FIG. 6 is a cross sectional view explaining the manufacturing step subsequent to the step of FIG. 5.

FIG. 7 is a cross sectional view explaining the manufacturing step subsequent to the step of FIG. 6.

FIG. 8 is a cross sectional view explaining the manufacturing step subsequent to the step of FIG. 7.

FIG. 9 is a cross sectional view explaining the manufacturing step subsequent to the step of FIG. 8.

FIG. 10 is a cross sectional view explaining the manufacturing step subsequent to the step of FIG. 9.

FIG. 11 is a cross sectional view explaining the manufacturing step subsequent to the step of FIG. 10.

FIG. 12 is a cross sectional view explaining the manufacturing step subsequent to the step of FIG. 11

FIG. 13 is a cross sectional view of a semiconductor device exhibiting a high breakdown voltage according to the third embodiment of the invention.

FIG. 14 shows the simulated distribution of the electric field strength (a) across the cross section (b) of the semiconductor device according to the third embodiment of the invention.

FIG. 15 is a cross sectional view of a semiconductor device exhibiting a high breakdown voltage according to the fourth embodiment of the invention.

FIG. 16(a) is a cross sectional view explaining a step for forming a plurality of impurity diffusion regions, the impurity concentrations thereof are different from each other.

FIG. 16(b) is a cross sectional view explaining the step for forming subsequent to the step of FIG. 16(a).

FIG. 16(c) is a cross sectional view explaining the step for forming subsequent to the step of FIG. 16(b).

FIG. 16(d) is a cross sectional view explaining the step for forming subsequent to the step of FIG. 16(c).

FIG. 16(e) is a cross sectional view explaining the step for forming subsequent to the step of FIG. 16(d).

FIG. 17(a) is a cross sectional view explaining a step for forming a plurality of impurity diffusion regions, the impurity concentrations thereof are different from each other, according to the fifth embodiment of the invention.

FIG. 17(b) is a cross sectional view explaining the step for forming subsequent to the step of FIG. 17(a).

FIG. 17(c) is a cross sectional view explaining the step for forming subsequent to the step of FIG. 17(b).

FIG. 17(d) is a cross sectional view explaining the step for forming subsequent to the step of FIG. 17(c).

FIG. 17(e) is a cross sectional view explaining the step for forming subsequent to the step of FIG. 17(d).

FIG. 18(a) is a cross sectional view explaining a step for forming a plurality of impurity diffusion regions, the conductivity types thereof are different from each other, according to the sixth embodiment of the invention.

FIG. 18(b) is a cross sectional view explaining the step for forming subsequent to the step of FIG. 18(a).

FIG. 18(c) is a cross sectional view explaining the step for forming subsequent to the step of FIG. 18(b).

FIG. 18(d) is a cross sectional view explaining the step for forming subsequent to the step of FIG. 18(c).

FIG. 19 is a cross sectional view of a semiconductor device including a p-type region formed of a plurality of regions, the impurity concentrations thereof are different from each other.

FIG. 20 is a cross sectional view of a semiconductor substrate with a plurality of masks formed thereon to form a p-type region including a plurality of regions, the impurity concentrations thereof are different from each other.

FIG. 21 is a cross sectional view of a conventional semiconductor device exhibiting a high breakdown voltage.

FIG. 22(a) is a cross sectional view for explaining the conventional ion implantation step for forming a p-type impurity diffusion region.

FIG. 22(b) is a cross sectional view for explaining the conventional thermal diffusion step for forming the p-type impurity diffusion region.

FIG. 23 is a cross sectional view of a conventional lateral power MOSFET exhibiting a high breakdown voltage and including the impurity diffusion region described with reference to FIGs. 22(a) and 22(b).

FIG. 24 shows an electric field strength distribution (a) in the cross section (b) of the conventional semiconductor device exhibiting a high breakdown voltage shown in FIG. 21.

[Assignment of the Reference Numerals]

1, 21: n-type silicon substrate
2: LTO-SiO_2 film
3: Plasma SiN film
4, 11, 25, 43: Photoresist
16, 46: Opening
5, 13, 26: Boron ion implantation

6, 12, 27: Boron ions
7, 83a, 159a, 169a: First p-type region
8, 83b, 159b, 169b: Second p-type region
9, 83c, 159c, 169c: Third p-type region
10, 14, 15, 22, 49: p-type region
23: SiO_2 film
24: SiN film
28: LOCOS
29: p^+-type region
30: Phosphorus ion implantation
31: Phosphorus ions
32: n^+-type region
41: Silicon substrate
42: SiO_2 film
44, 100, 200: Photomask
45, 101, 201: Ultraviolet ray
47: Ion implantation
48: Ions
71: n-type silicon substrate
83: p-type offset region
87: p-type region (p-type base region)
88: n-type source region
89: n-type drain region
90: p^+-type contact region
91, 163: Gate insulation film
92, 157: Gate electrode
93, 160: Insulation film
94, 161: Source electrode
95, 162: Drain electrode
151: p-type substrate

152, 164: n-type well region

153: p-type base region

154: n-type drain region

155: n-type source region

156: p^+-type contact region

158, 168: Boron diffusion depth

159, 169: p-type diffusion layer (p-type offset region)

165: First n-type well region

166: Second n-type well region

167: Third n-type well region

[Document Title] ABSTRACT

[Abstract]

[Object]

To provide a semiconductor device exhibiting a stable and high breakdown voltage, that is manufactured with low manufacturing costs, to provide the method of manufacturing the semiconductor device and to provide the method of forming a plurality of impurity diffusion regions in the semiconductor device.

[Configuration]

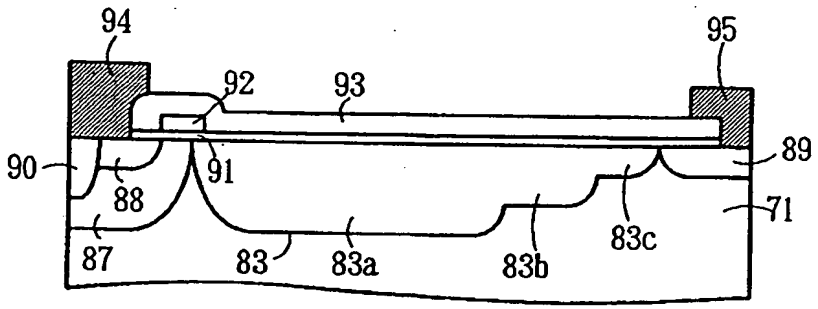
The semiconductor device exhibiting a high breakdown voltage according to the invention includes an n-type silicon substrate 71; a p-type base region 87 in the surface portion of substrate 71; an n-type drain region 89 in the surface portion of n-type substrate 71; a p-type offset region 83 in the surface portion of n-type substrate 71; an n-type source region 88 in the surface portion of p-type base region 87; a p-type contact region 90 in the surface portion of p-type base region 87; a gate electrode 92 above the extended portion of p-type base region 87 extended between n-type source region 88 and n-type substrate 71 (or p-type offset region 83) with a gate insulation film 91 interposed therebetween; an insulation film 93 on gate electrode 92 and p-type offset region 83; a source electrode 94 on n-type source region 88; and a drain electrode 95 on n-type drain region 89. The p-type offset region 83 is formed of a first p-type region 83a, the impurity concentration thereof is the highest and the diffusion depth thereof is the deepest; a second p-type region 83b, the impurity concentration and the diffusion depth thereof are intermediate; and a third p-type region 83c, the impurity concentration thereof is the lowest and the diffusion depth thereof is the shallowest.

[Selected Drawing] FIG. 1

[書類名] 図面 Document Title: Drawings

[図1]

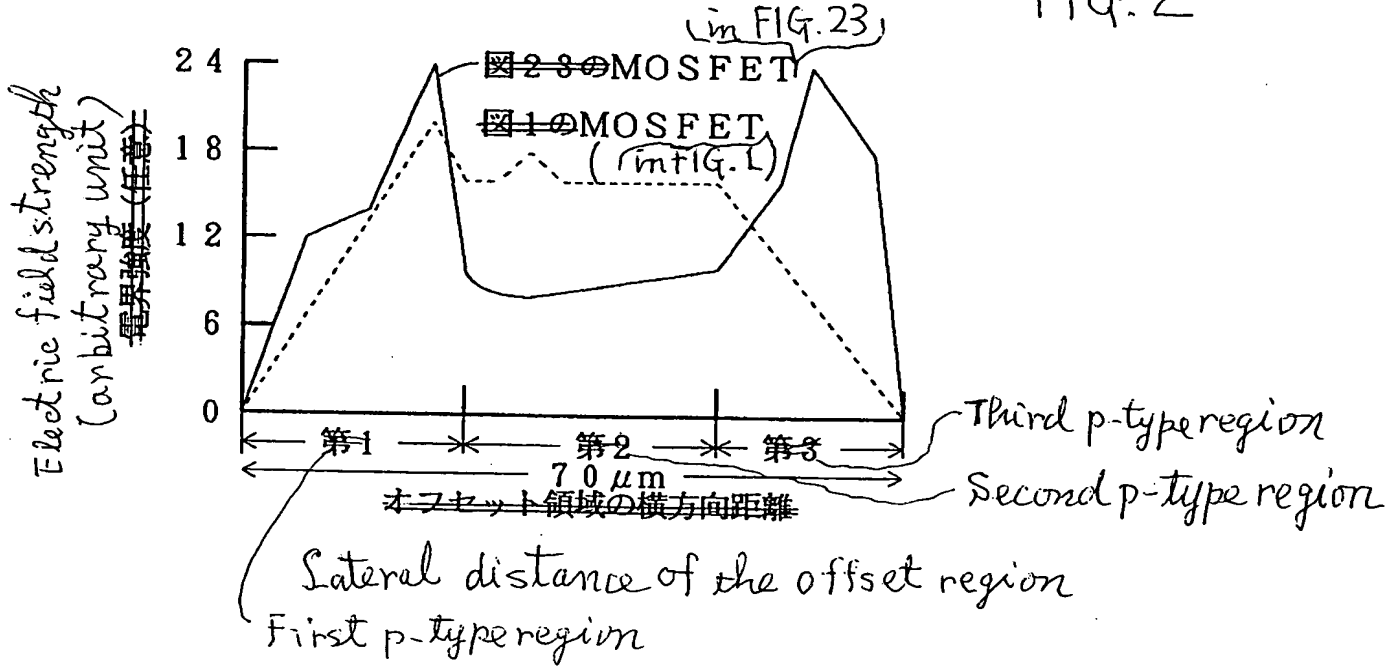
FIG. 1



71・・・nシリコン基板
83・・・pオフセット領域
83a ・・第1p領域
83b ・・第2p領域
83c ・・第3p領域
87・・・p領域（pベース領域）
88・・・nソース領域
89・・・nドレイン領域
90・・・p^+コンタクト領域
91・・・ゲート絶縁膜
92・・・ゲート電極
93・・・絶縁膜
94・・・ソース電極
95・・・ドレイン電極

[図2]

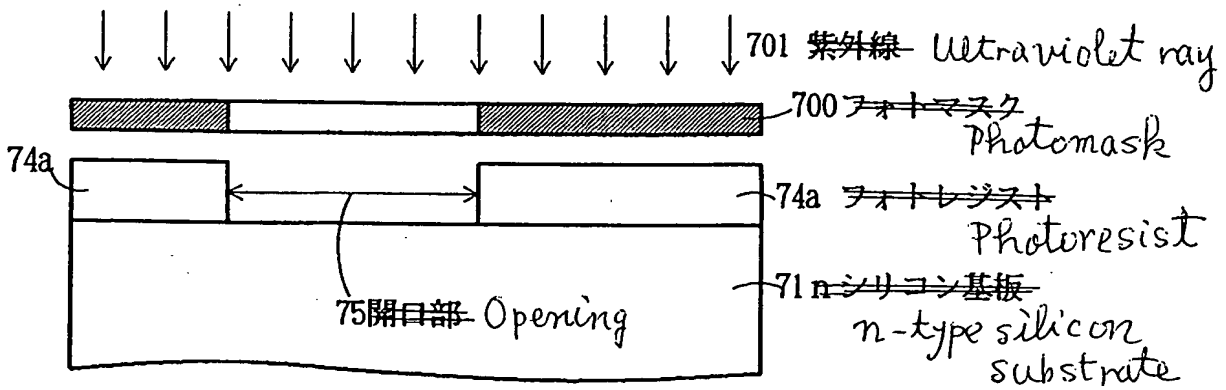
FIG. 2



71: n-type silicon substrate
83: p-type offset region
83a: First p-type region
83b: Second p-type region
83c: Third p-type region
87: p-type region (p-type base region)
88: n-type source region
89: n-type drain region
90: p^+-type contact region
91: Gate insulation film
92: Gate electrode
93: Insulation film
94: Source electrode
95: Drain electrode

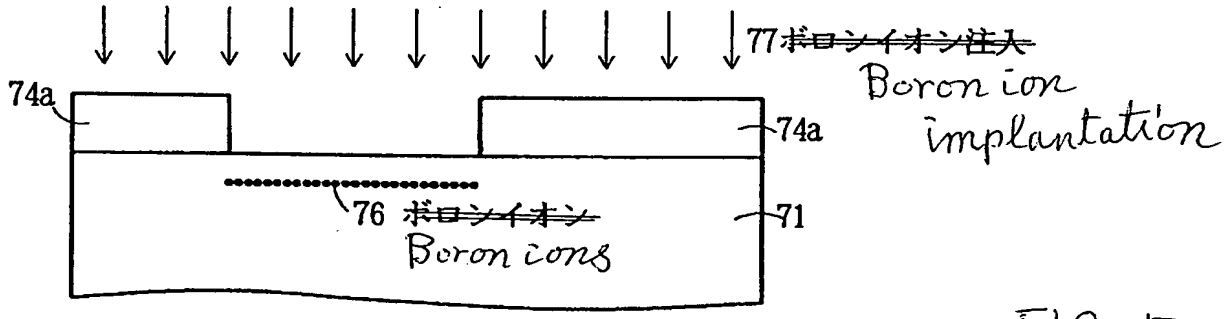
[図3]

FIG. 3



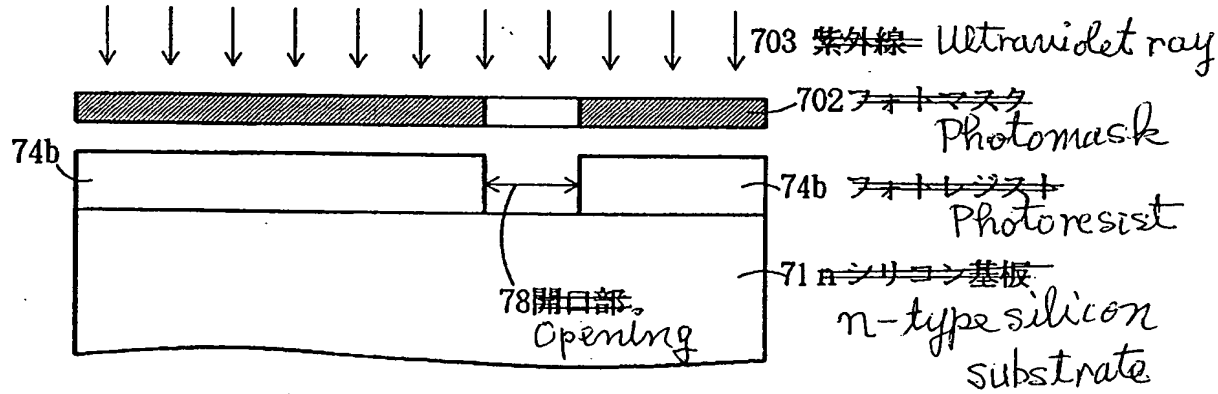
[図4]

FIG. 4



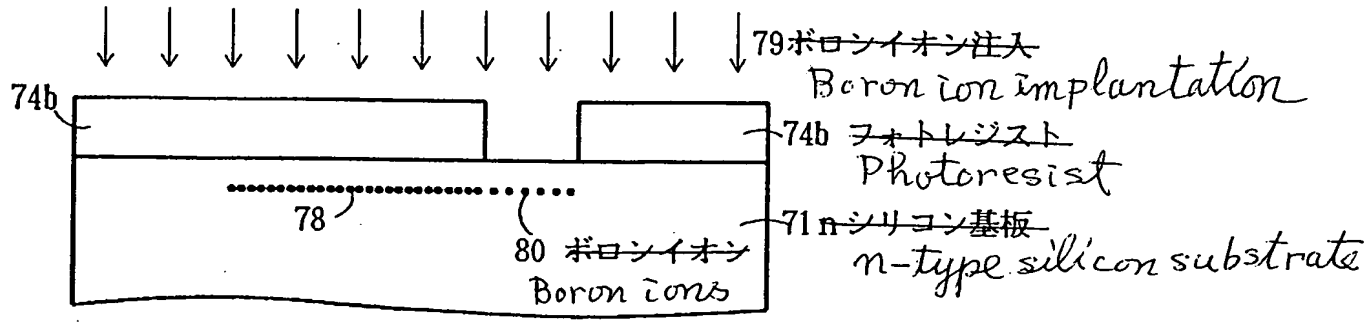
[図5]

FIG. 5



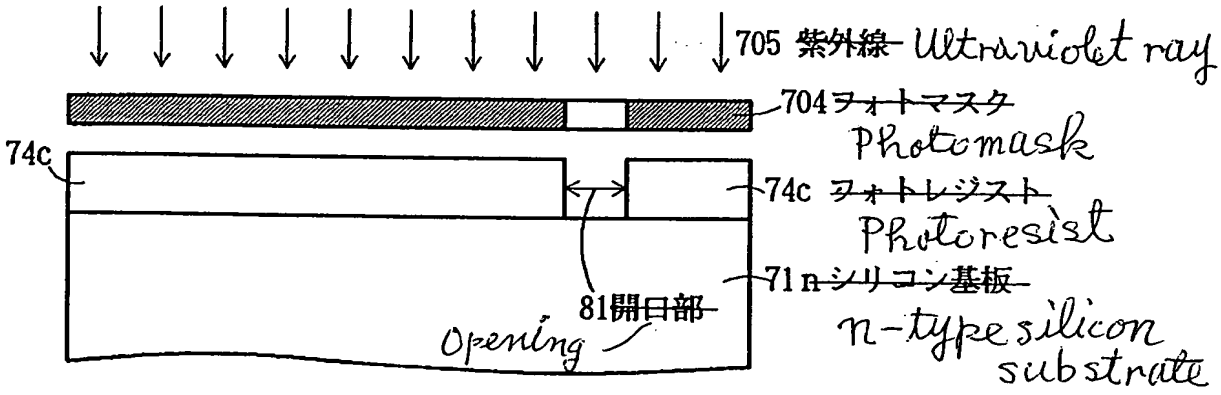
~~[図6]~~

FIG. 6



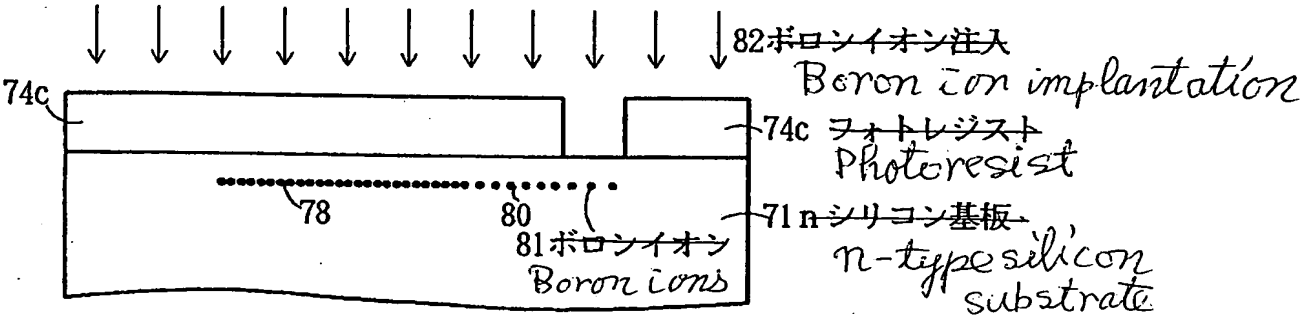
~~[図7]~~

FIG. 7



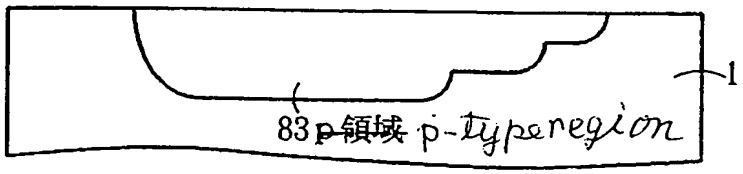
~~[図8]~~

FIG. 8



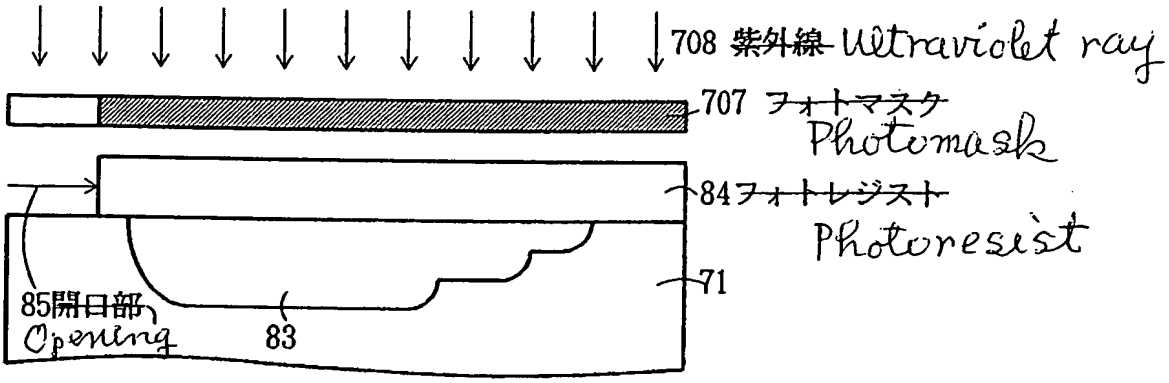
~~[図9]~~

FIG. 9



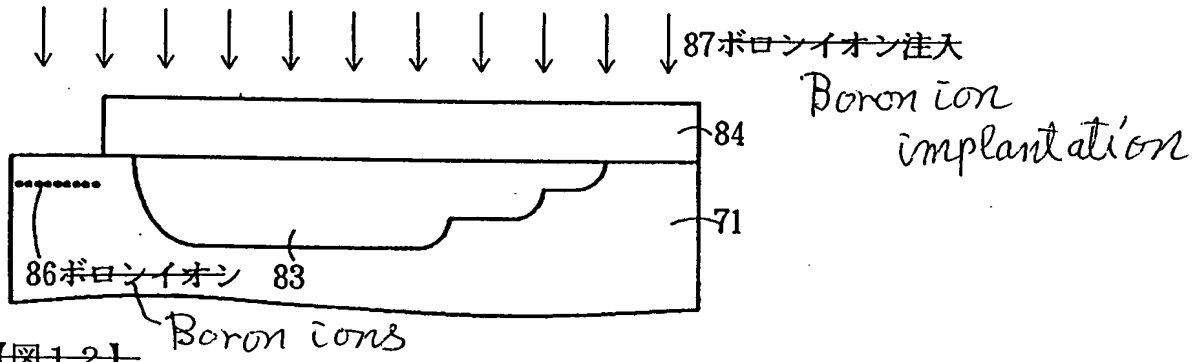
~~[図10]~~

FIG. 10



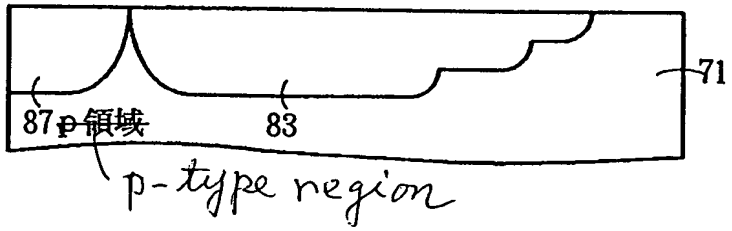
~~[図11]~~

FIG. 11



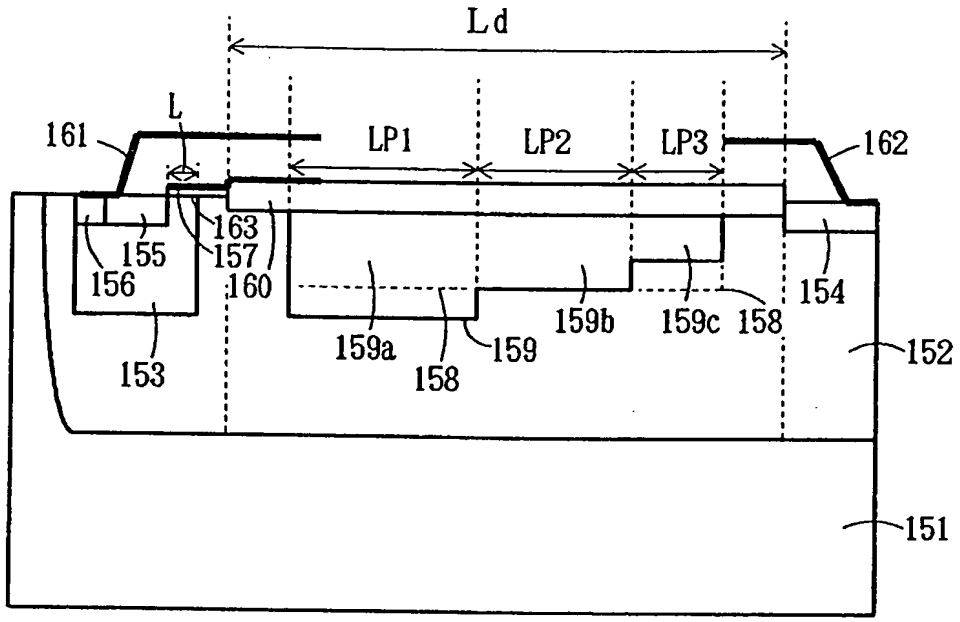
~~[図12]~~

FIG. 12



~~[図13]~~

FIG. 13

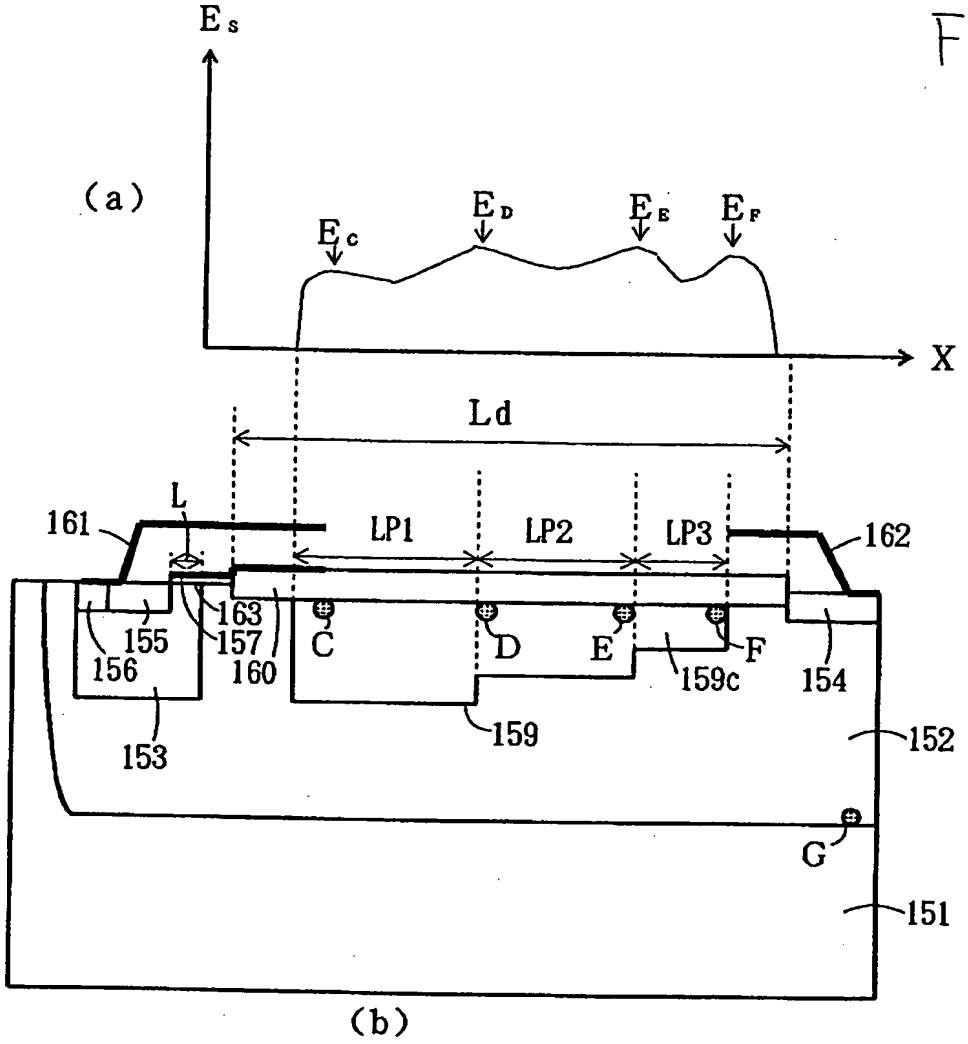


151・・・p基板
152・・・nウエル領域
153・・・pベース領域
154・・・nドレイン領域
155・・・nソース領域
156・・・p^+ コンタクト領域
157・・・ゲート電極
158・・・ボロン拡散深さ
159・・・p拡散層（pオフセット領域）
159a ・・第1p領域
159b ・・第2p領域
159c ・・第3p領域
160・・・絶縁膜
161・・・ソース電極
162・・・ドレイン電極
163・・・ゲート絶縁膜

151: p-type substrate
152: n-type well region
153: p-type base region
154: n-type drain region
155 n-type source region
156: p^+-type contact region
157: Gate electrode
158: Boron diffusion depth
159: p-type diffusion layer (p-type offset region)
159a: First p-type region
159b: Second p-type region
159c: Third p-type region
160: Insulation film
161: Source electrode
162: Drain electrode
163: Gate insulation film

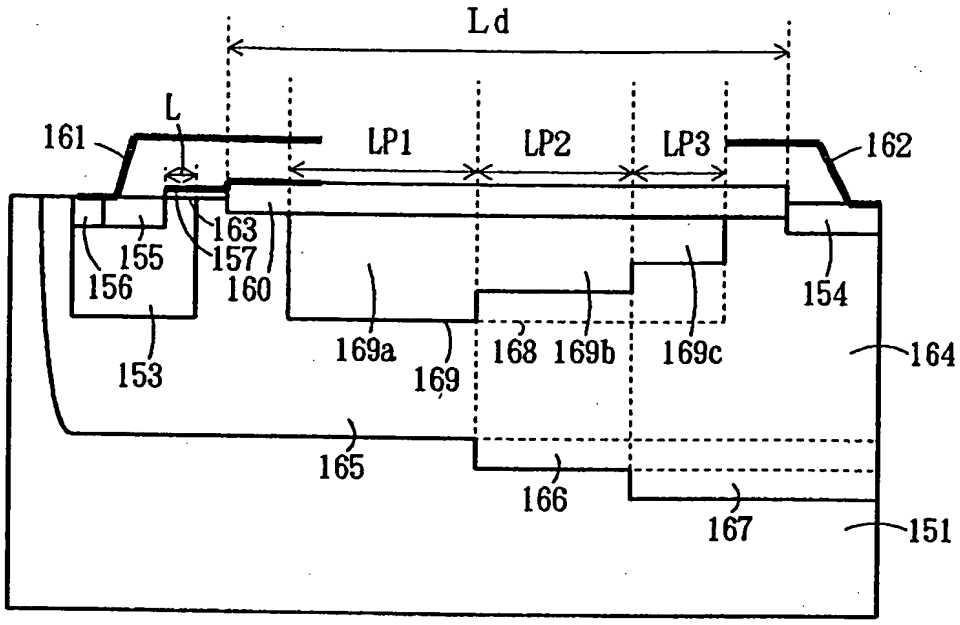
[図14]

FIG.14


Es
(a)
Ec
ED
EE
EF
X
Ld
L
161
LP1
LP2
LP3
162
163
155
157
156
160
C
D
E
F
159c
154
159
153
152
G
151
(b)

[図15]

FIG. 15



164・・・nウエル領域
165・・・第1nウエル領域
166・・・第2nウエル領域
167・・・第3nウエル領域
168・・・ボロン拡散深さ
169・・・p拡散層
169a ・・第1p領域
169b ・・第2p領域
169c ・・第3p領域

⇨

164: n-type well region
165: First n-type well region
166: Second n-type well region
167: Third n-type well region
168: Boron diffusion depth
169: p-type diffusion layer
169a: First p-type region
169b: Second p-type region
169c: Third p-type region

【図16】

FIG.16(a)

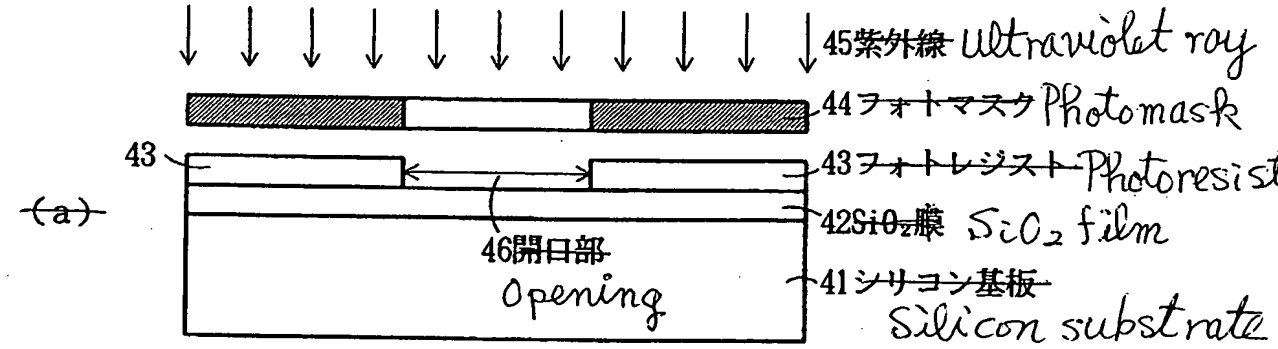


FIG.16(b)

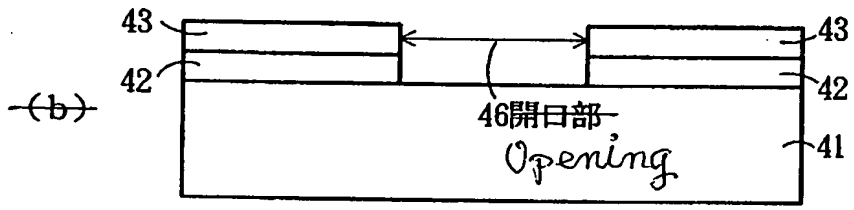


FIG.16(c)

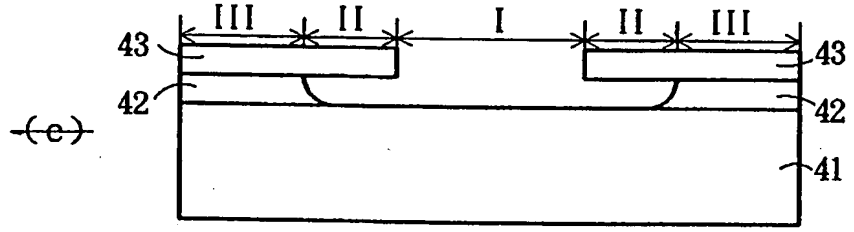


FIG.16(d)

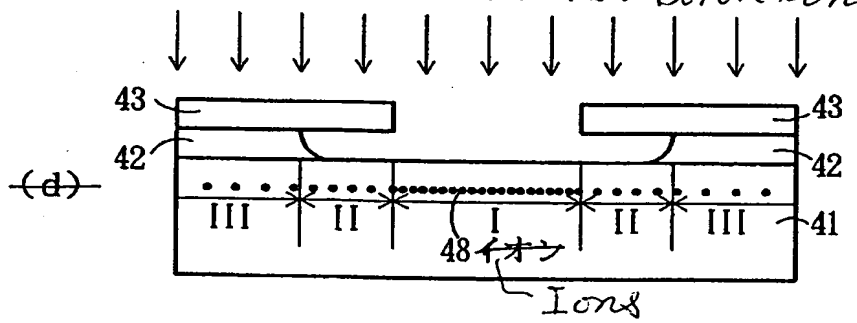
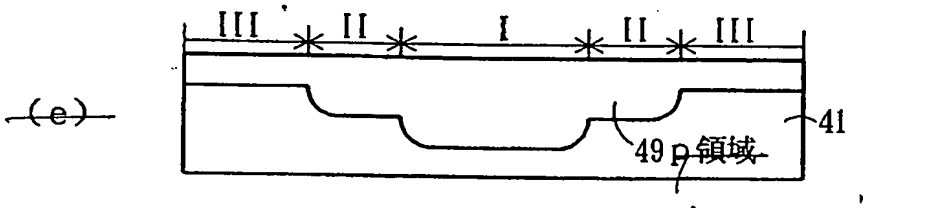


FIG.16(e)



【図17】

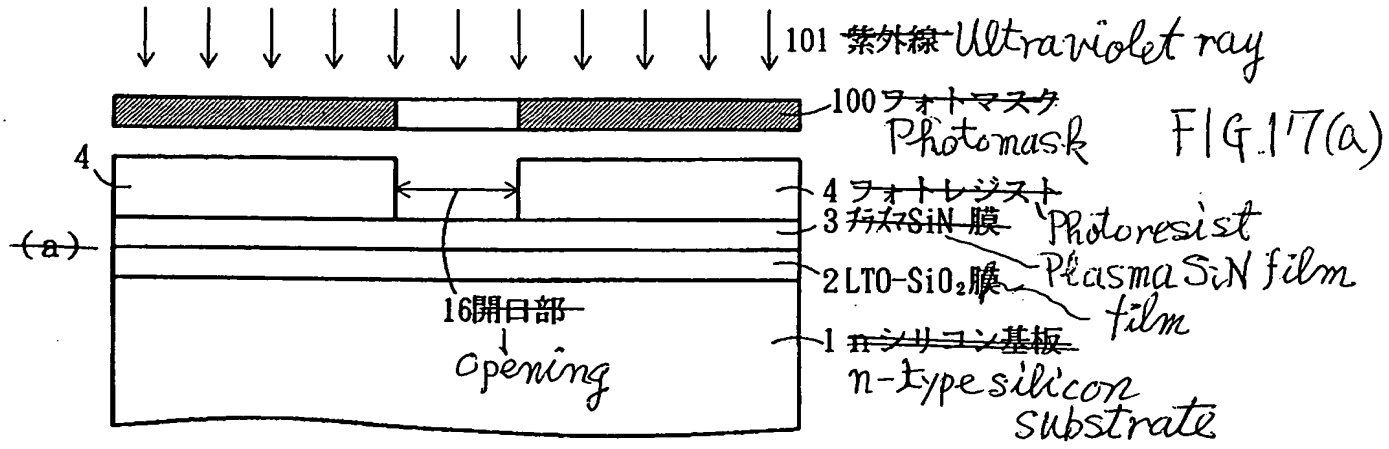


FIG.17(a)

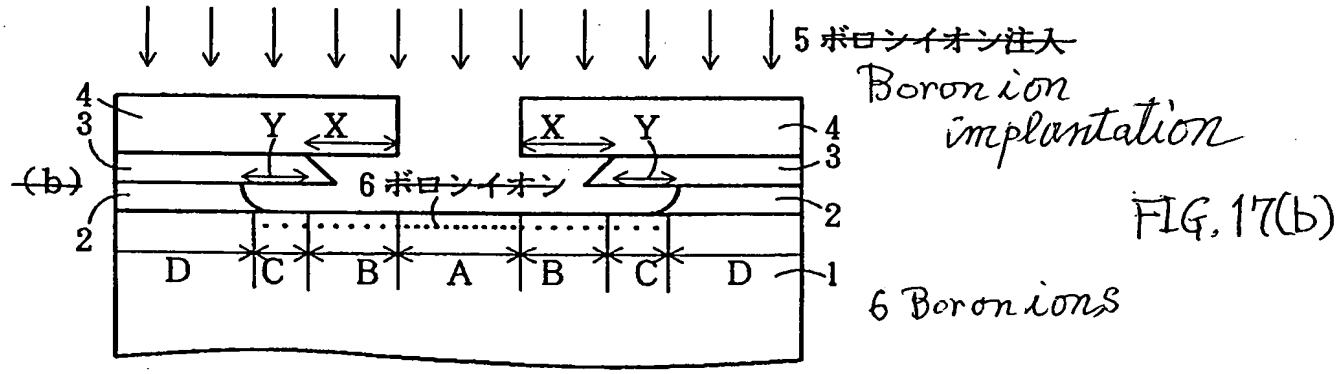


FIG.17(b)

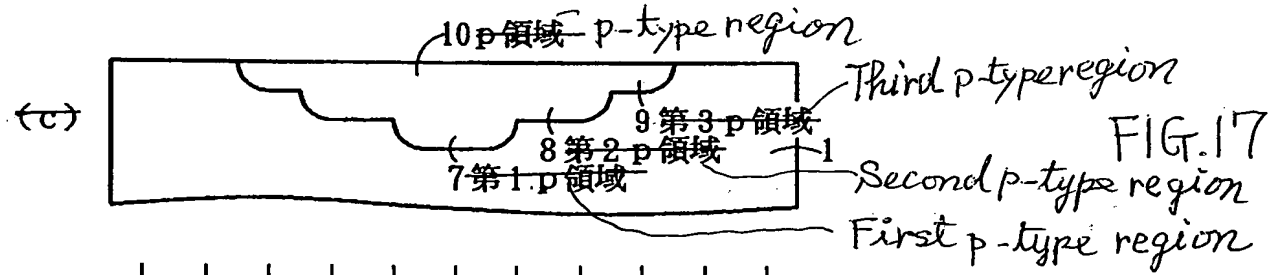


FIG.17(c)

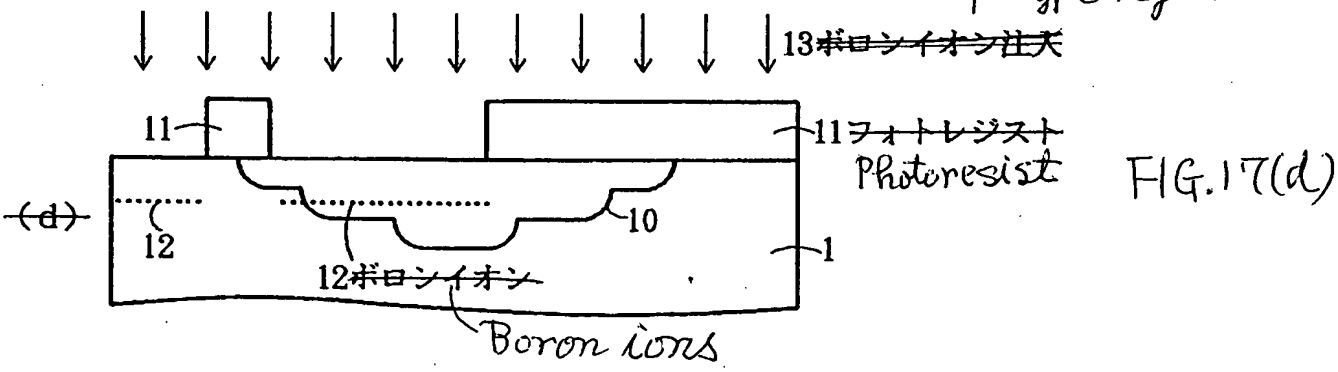


FIG.17(d)

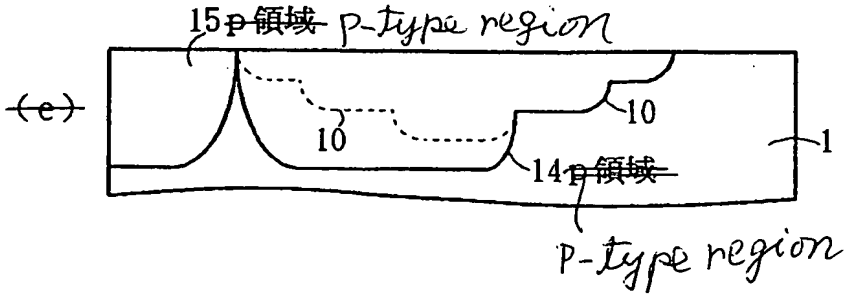


FIG.17(e)

~~【図1-8】~~

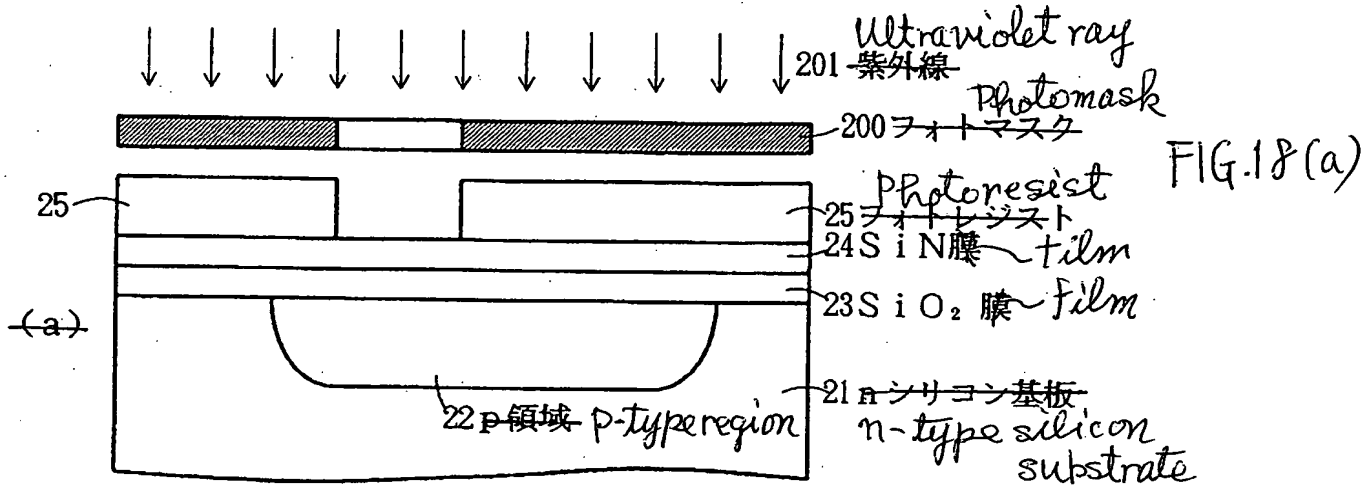


FIG.18(a)

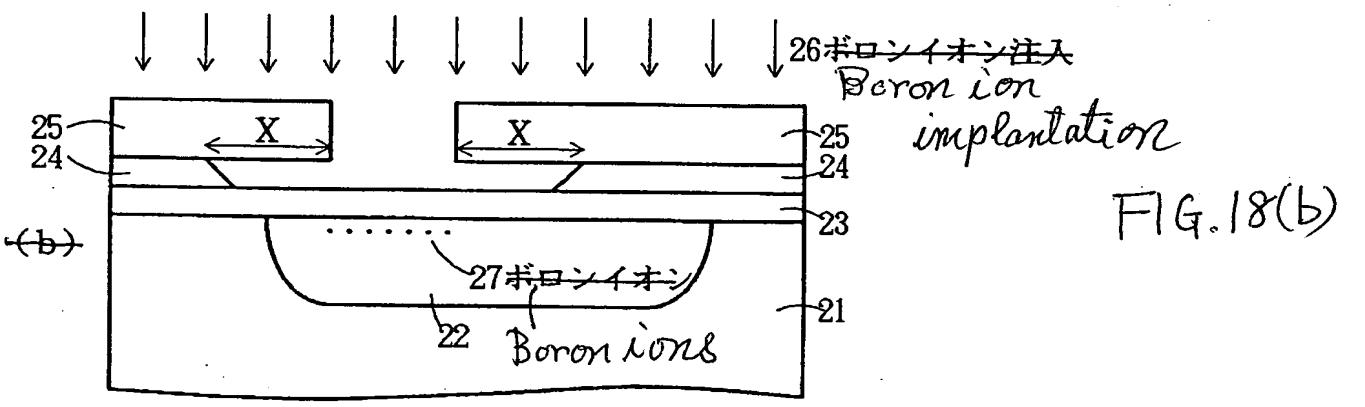


FIG.18(b)

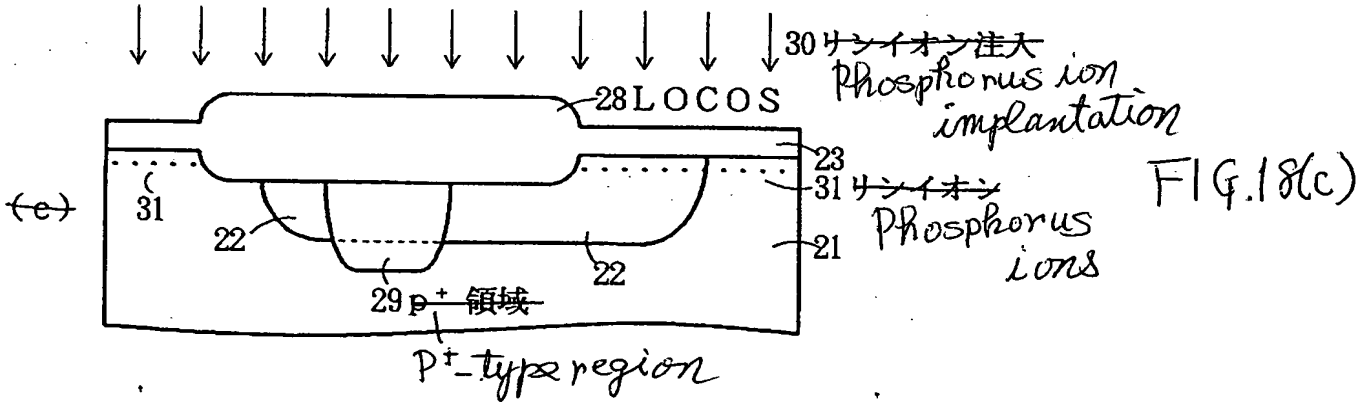


FIG.18(c)

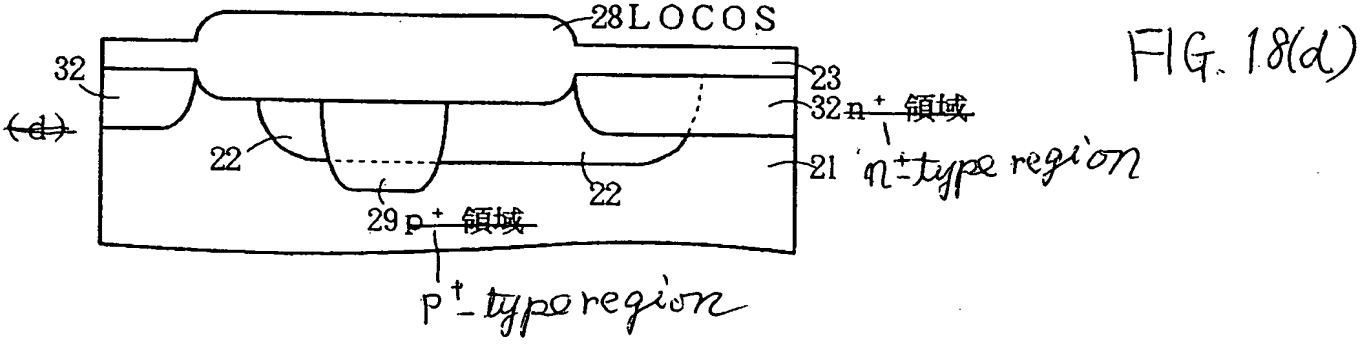
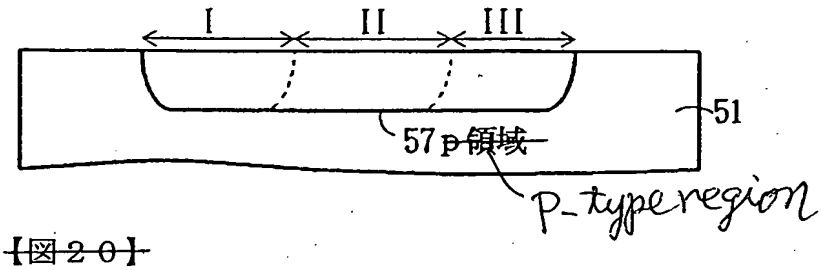


FIG.18(d)

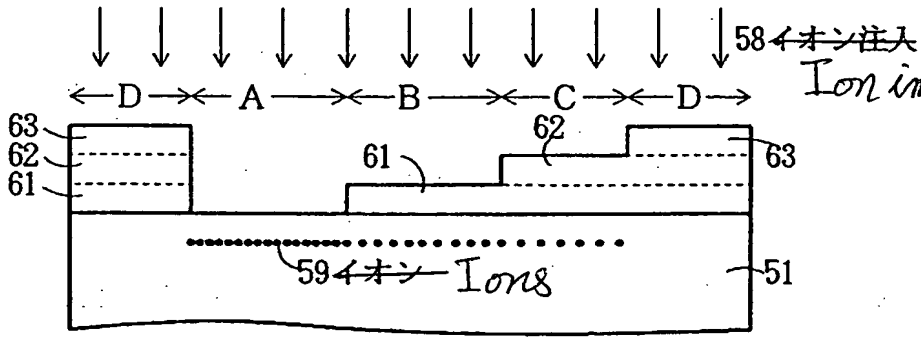
【図19】

FIG. 19



【図20】

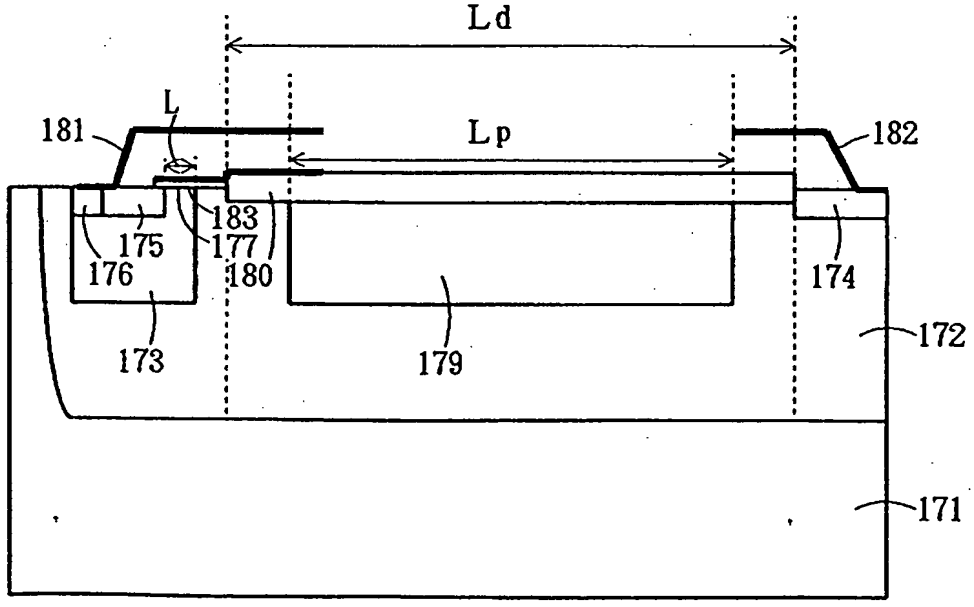
FIG. 20



61, 62, 63 ・・・ イオン注入マスク
Masks for ion implantation

【図21】

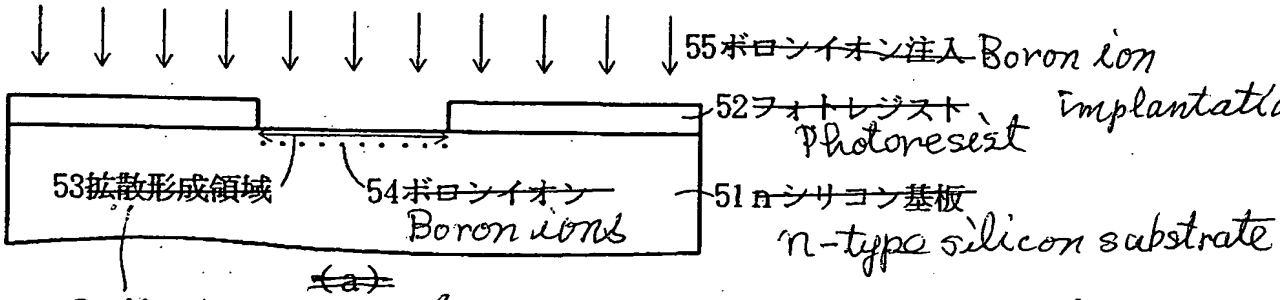
FIG. 21



171: p-type substrate
172: n-type well region
173: p-type base region
174: n-type drain region
175: n-type source region
176: p^+-type contact region
177: Gate electrode
179: p-type diffusion layer (p-type offset region)
180: Insulation film
181: Source electrode
182: Drain electrode
183: Gate oxide film

【図２２】

FIG. 22(a)



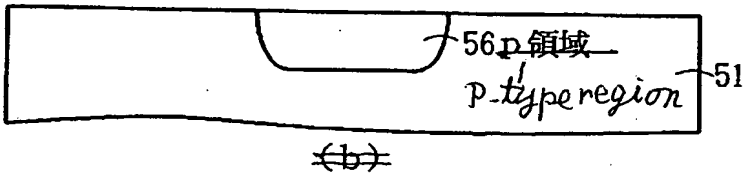
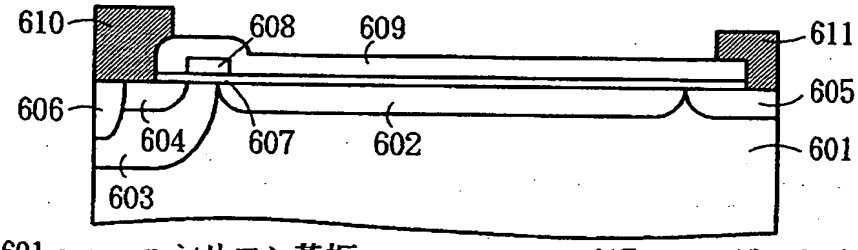


FIG. 22(b)

【図２３】

FIG. 23



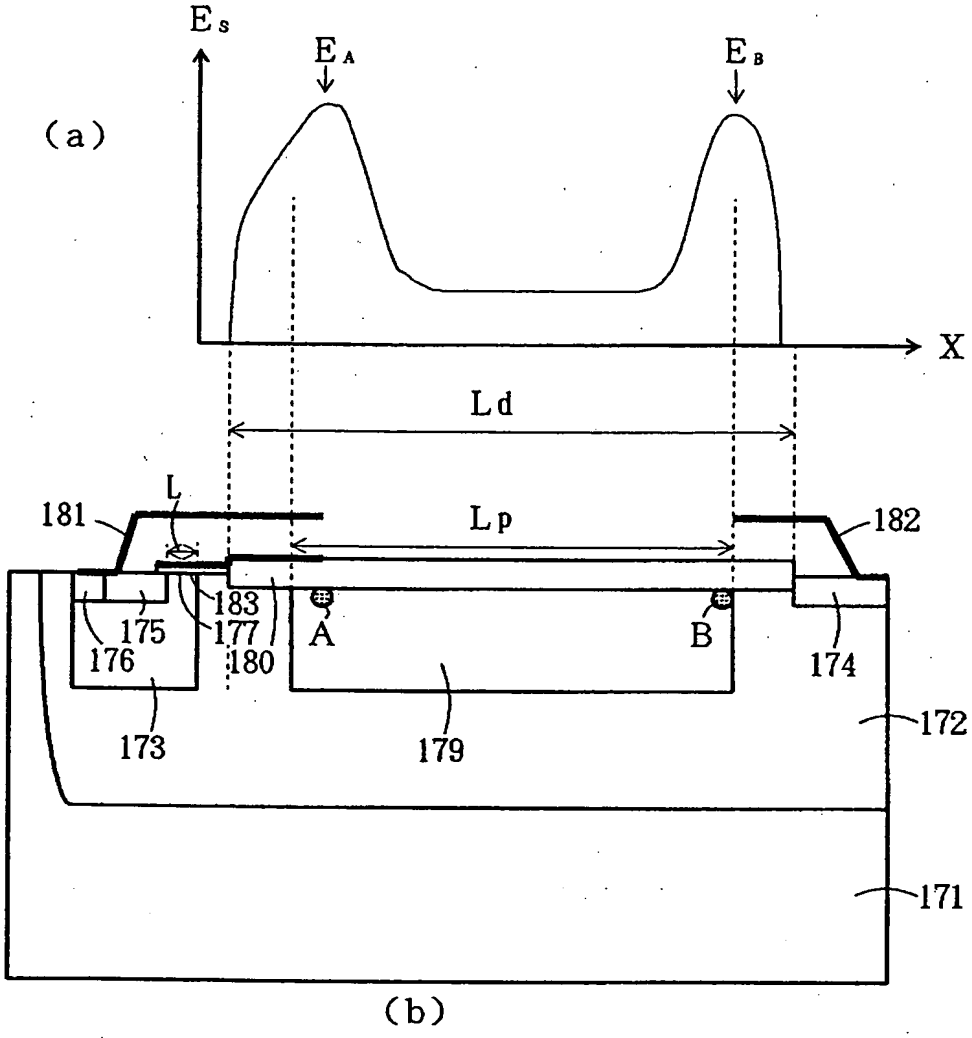
601・・・nシリコン基板
602・・・p領域（pオフセット領域）
603・・・p領域（pベース領域）
604・・・nソース領域
605・・・nドレイン領域
606・・・pコンタクト領域
607・・・ゲート酸化膜
608・・・ゲート電極
609・・・絶縁膜
610・・・ソース電極
611・・・ドレイン電極

⇩

601: n-type silicon substrate
602: p-type region (p-type offset region)
603: p-type region (p-type base region)
604: n-type source region
605: n-type drain region
606: p-type contact region
607: Gate oxide film
608: Gate electrode
609: Insulation film
610: Source electrode
611: Drain electrode

[図24]

FIG. 24


Es
EA
EB
(a)
X
Ld
L
Lp
181
182
183
175
177
176
180
A
B
174
173
179
172
171
(b)